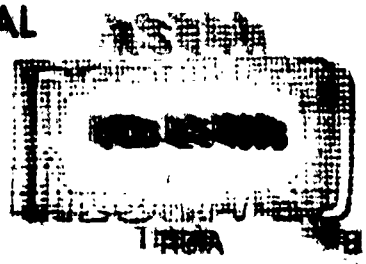
PREPARED UNDER

BUREAU OF NAVAL WEAPONS
DEPARTMENT OF THE NAVY

CONTRACT NO. NOw 62-0984-d

VOLTAGE REGULATION AND CONVERSION

IN UNCONVENTIONAL ELECTRICAL GENERATOR SYSTEMS



QUARTERLY REPORT
NUMBERS 1 AND 2 COMBINED
JULY 30, 1962

DIRECT ENERGY CONVERSION OPERATION
GENERAL ELECTRIC
930 WESTERN AVE., WEST LYNN, MASS.

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CONTENTS

1.0 ABSTRACT

The technical progress during the first two quarters of activity (January 1, 1962 to July 1, 1962) on the study of voltage regulation and conversion in unconventional electrical generator systems (Contract NO_w-62-0984-D) for the Bureau of Naval Weapons is presented in this report. The approach and work plans for the complete study are given. The progress to date in developing a light weight efficient DC to DC circuit known as the "Flyback Circuit" is included. Information giving the results to date in a high frequency switching investigation aimed at reducing circuit weight is presented. A discussion of power transistor characteristics pertinent to voltage conversions circuits is included. Design data permitting the design of a minimum weight inductor or transformer for any given power loss is given.

2.0 PURPOSE OF PROJECT

In recent years, unconventional power sources have been developed to a degree where they are becoming practical power sources for many military and space applications. In many of these, closely regulated power at 28 volts DC or at higher 400 cps AC voltages is required. During this time, only a small amount of attention has been given to the electrical system problems associated with the use of these generating devices. These problems include that of close control of the output voltage with load variation, compatibility of the dynamic characteristics of the generator with a load, and the problem of converting to AC power where needed.

During the same period, great strides have been made in the solid state device technology. Devices such as the silicon-controlled rectifier and the large power transistor now make possible the development of static voltage regulation-conversion circuits with much higher efficiency and reliability than previously attainable. Only recently has any significant effort been devoted to the development of such solid state circuits for use with unconventional electrical power sources. Instead, the emphasis has been on the commercial and aircraft electrical system applications.

The purpose of this study is to investigate methods of controlling voltage in or at the power source; to show feasibility of advanced external voltage conversion and regulator circuits aimed specifically at use with unconventional power sources; to investigate the system problems connected with the use of static external voltage converters and unconventional power sources; to determine the most desirable systems to use; and to establish the performance characteristics of these systems.

The overall investigation was begun in June 1960, under Contract $NO_w 60-0824-C$. That contract expired in December, 1961. The work under the present contract is a continuation of that effort.

3.0 PROJECT ORGANIZATION AND PERSONNEL

The work effort has been organized and divided in such a manner as to insure maximum utilization of the technical resources of the General Electric Company. The overall responsibility and technical direction of the program rests with the Direct Energy Conversion Operation (DECO) of the Ordnance Department located in Lynn, Mass. In addition, DECO is conducting the power source investigation portion of the total study. The services of sister Departments and company laboratories such as the Research Laboratory and the General Engineering Laboratory are being obtained as deemed beneficial for the program.

A large part of the external voltage conversion and regulation portion of the study is being performed at the General Engineering Laboratory (GEL) in Schenectady, New York. DECO is also performing a small portion of this work. In this case, also the assistance of sister Departments and laboratories is being obtained when a significant contribution can be made.

The systems portion of the study is being performed at DECO with the assistance of the General Engineering Laboratory.

This project is under the overall direction of Mr. C.C. Christianson, Project Engineer, Direct Energy Conversion Operation, at the Lynn River Works.

The principal contributors to this Progress Report are as follows:

Direct Energy Conversion Operation - C.C. Christianson

General Engineering Laboratory - R. L. Maul
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4.0 TECHNICAL PROGRESS - POWER SOURCES INVESTIGATION

4.1 Resume'

The work plans and progress to date in the power sources investigation are reported herein. This portion of the study is devoted to a determination of the basic electrical characteristics of the unconventional power sources. In addition, it is concerned with the establishment of methods of directly regulating and controlling the output voltage of these unconventional power sources.

Item 4.2 summarizes the approach and work plans to be followed in conducting the power source investigation. The individual tasks are indicated along with the work to be performed and the results desired.

To date, effort in this area has been limited to a detail planning of each of the tasks. Work has begun on a study of fuel cell dynamic electrical characteristics. However, the progress to date is not sufficient to warrant reporting it here.

4.2 Approach and Work Plans

The power sources investigation consists of four major tasks. These are:

a. Study of fuel cell dynamic electrical characteristics.
b. Transient energy storage study.
c. Voltage control by series-parallel switching.
d. Miscellaneous unconventional power source study.

These tasks are discussed in detail in the following paragraphs.

4.2.1 Fuel Cell Dynamic Electrical Characteristic Study

A knowledge of the electrical performance of a fuel cell under all transient conditions is essential in order to be able to do an adequate electrical system design. For example, practically all efficient external voltage converters impose a pulsating load on the power source. The degree of filtering required at the input to the external voltage converter is dependent upon the internal impedance of the power source at the pulsating frequency. In addition, it is desirable that the transient voltage response resulting from a load change be known.

In particular, the behavior of a power source during faults or momentary over-loads is important. In fact, it is important that the power source be represented by a general mathematical model, which will describe the performance of the power source under all conditions, both transient and steady state. This general mathematical model may be a variety of forms, the most common being either an equivalent electrical circuit or a block diagram.

Such a general mathematical model is not presently available for a fuel cell. It is the goal of this task to arrive at a mathematical model for an ion exchange membrane fuel cell. A preliminary investigation of this type was carried on under the previous contract (Contract NO_w60-0824-C). This task is a large extension of that effort.

A combined analytical and experimental approach will be used to arrive at the mathematical model of the fuel cell. Test data will be obtained which gives the differential output impedance at various DC loads and/or load disturbance frequencies between 0 and approximately 100,000 cps. The resultant differential output impedance information will be used to synthesize the electrical model of the fuel cell. The validity of the resultant electrical model will be checked by comparing its predicted response to various load disturbances (short circuits, step load changes, reverse currents, etc.) with those measured from an actual fuel cell. In addition, an attempt will be made to correlate the characteristics of the mathematical model with the physical parameters of the fuel cell.

4.2.2 Transient Energy Storage Study

The results of the previous study (Contract NO_w60-0824-C) indicated that one of the more desirable methods of control of output voltage of both thermoelectric and thermionic generators is the variation of an appropriate temperature as load varies. In the case of a thermoelectric source for example, the output voltage can be closely controlled by effectively varying the source temperature which results in a variation in the temperature drop across the thermoelectric elements. Thus, if the electrical load were reduced, the source temperature would also be reduced resulting in a smaller temperature drop across the thermoelectric elements and a constant output voltage.

Unfortunately, however, voltage control by temperature variation has the disadvantage of slow transient response. The time constants involved in changing from one temperature to another are typically 15 to 60 seconds. Such a slow response in the change in the electrical load capability is generally intolerable. However, this disadvantage could be overcome if the required transient electrical power were delivered from some energy accumulator such as a secondary battery which would supply electrical energy during increasing load transients and would be recharged from the regular power source during steady state operation.

Another need for transient energy storage occurs in applications where the normal average power is relatively small compared with occasional peak power loads. In such cases, the optimum system may well be a design in which the primary source delivers the average power, and the power peaks are borne by a secondary battery.

The purpose of this task is to establish methods of supplying the transient energy required to maintain output voltage during momentary peak loads or during transient load changes. The performance capabilities and limitations of various transient energy storage methods will be determined with emphasis on secondary batteries. Various systems utilizing the best transient energy storage methods will then be synthesized and evaluated. Performance characteristics (weight, volume, efficiency, etc.) and limitations will be determined.

4.2.3 Voltage Control by Series - Parallel Switching

The results of the previous study (Contract NO_w-60-0824-C0 indicated that one very attractive method of output voltage control of an unconventional power source involves changing the number of individual power source units in series or parallel as the load varies. This can be accomplished by using an appropriate circuitry in which transistors serve both as selector switches and as variable resistances. Good voltage control and high efficiency can be obtained with only a small penalty in weight of the circuitry required.

The purpose of this task is to develop the circuitry and demonstrate this method of voltage control on a fuel cell type of power source. The task includes synthesis of various circuits, evaluation of these circuits, and selection of the optimum circuit. The selected optimum circuit will then be developed and used to demonstrate the feasibility of this method of voltage control.

4.2.4 Miscellaneous Unconventional Power Source Study

In the previous study (Contract NO_w60-0824-C) the electrical characteristics of thermoelectric, thermionic, and fuel cell generators were established. In addition, various methods of voltage control of these sources were evaluated. The purpose of the present task is two-fold. First, the electrical characteristics and voltage control possibilities of such forthcoming unconventional power sources is the Aerosol generator, thermal galvanic generators and other new energy sources will be determined. Secondly, the electrical characteristics of thermoelectric, thermionic, and fuel cell generators will be kept up to date by factoring in the advances in these power source technologies. In addition, an attempt will be made to determine the electrical characteristics of fuel cells other than the ion exchange membrane type cell.

5.0 TECHNICAL PROGRESS - EXTERNAL VOLTAGE CONVERSION AND REGULATION

5.1 Resume'

A summary of the technical effort in the area of external voltage conversion and regulation is given in this section. The section has been divided as follows:

5.2 Approach and Work Plans
5.3 Flyback Circuit Development
5.4 High Frequency Switching Investigation
5.5 Advance Semiconductor Investigation
5.6 Advanced Circuit Concept Study

Item 5.2 consists of a general discussion of the technical work approach and plans for the external voltage conversion and regulation portion of the overall study. The influence of the external voltage conversion devices on the system approach of providing static, low weight, and low loss power systems incorporating unconventional energy conversion generators is discussed.

Item 5.3 is a report of the work associated with the development of the "Flyback" circuit which has a potential of providing a low weight, high efficiency, DC-DC converter. Analytical evaluation has indicated a converter weight density of 35 lbs/kw at a power output of 75 watts, and a full load input voltage of 9.0 volts DC is feasible. A theoretical analysis of the power circuit is presented along with design equations for selecting major circuit components. Several modes of operation are investigated and presented. Initial control circuit problems associated with driving the power transistor in a switching mode are discussed. Preliminary results have indicated a change was needed in the saturable current transformer drive circuit for the power transistor.

Item 5.4 is a report of the effort associated with high frequency switching conversion circuits. The concept of switching power transistors at frequencies in excess of 5 kilocycles per second offers a way to reduce the size and weight of electromagnetic components which comprise a major part of the total circuit weight. The initial effort reported here is devoted to a study of the relationships between magnetic core material, core configurations, core losses, and power handling capability as a function of frequency.

This effort is required to determine engineering design equations and analytical expressions for the purpose of selecting a feasible or practical operating frequency. Although a reduction in core material (for a given flux density) is achieved at increased frequencies, core losses increase and it is imperative to optimize frequency with respect to both weight and efficiency. As such, a comprehensive investigation of magnetic component performance initiates the effort directed toward high frequency switching techniques in power conversion circuits.

Section 5.5 is a report of the progress to date associated with the effort on advanced semiconductors. A preliminary study of transistor notation with respect to rating and characteristics is presented. The study is directed at those characteristics and ratings which are related to the operation of transistors in the switching mode. The operation of the power transistor with respect to applied voltage and current polarity is illustrated for the distinct regions of transition from the non-conducting state to the conducting state.

A survey of commercially available devices is presented and documented. This work represents an initial effort in obtaining devices which will minimize those losses associated with switching devices.

Item 5.6 summarizes the effort to date in the advanced circuit concept study. The purpose of this effort is to determine quantitatively the basic concepts of circuit construction which lead to low weight, highly efficient circuits. These concepts will be used to synthesize advanced circuits which will then be evaluated. The results of the effort of the past report period in establishing design curves for minimum weight inductors and transformers is reported herein.

5.2 Approach and Work Plans

5.2.1 Introduction

At the conclusion of the previous study (Contract Number NO_w-60-0824-C) of voltage regulation and power stability in unconventional electrical generator systems, it was possible to formulate and assess static power conversion techniques on an individual basis as well as on a system basis.

The system basis included the unconventional energy converter (fuel cell, thermionic, thermoelectric), combined with external circuitry whose function was to convert the source voltage to a desired DC or AC level and regulate the voltage overstated load conditions. A major factor is the total system weight. It was found that for any given application, the weight of the primary power source and fuel is dependent upon the power which must be supplied to the input of the voltage converter which is in turn a function of the voltage converter efficiency. As the voltage converter efficiency is increased, the primary power source weight is reduced. However, if the voltage converter efficiency is increased beyond an optimum point, the voltage converter weight will increase faster than the source weight decreases.

From the above discussion, one conclusion is somewhat evident. An increase in voltage converter efficiency at the expense of weight must be justified on a system basis taking into consideration the desired system parameters, such as power output rating, desired output voltage and available source voltage. It is highly desirable to find means of voltage converter efficiency at little or no sacrifice in circuit weight per given power output rating.

In the previous study, it was apparent that certain functions are necessary before a low D-C voltage can be transformed to a higher level D-C or A-C voltage efficiently. The simple technique of achieving the desired voltage by inserting either series or parallel impedance in the power circuit cannot be tolerated because of the inherently high internal impedance of the prime power source. Sources with a regulation in the order of 100% would require a loss of 50% power in a series dissipating resistor. The net result is then a "lossy" method of regulation with no way of providing voltage step-up. One of the most successful and efficient voltage conversion means requires the chopping of a D-C source voltage to produce a time varying current which in turn produces a magnetic flux which changes as a function of time. Once a time varying flux is available, transformation can be achieved within well-defined and known techniques. Regulation of the output voltage, however, is still a problem and it requires a separate and distinct circuit function.

With the information generated in the previous study, it was possible to define those areas which limit power conversion circuit performance. These areas are reflected in the planned program which is discussed in the subsequent sections.

5.2.2 Flyback Circuit Development

During the course of the previous study, a DC-DC conversion circuit was investigated which has the potential of being light weight (35 lb/kw at 75 watts rated output) at a full load efficiency of 90% or greater. The purpose of this task is to design and construct a DC-DC voltage converter using a "flyback" circuit. The model circuit will demonstrate optimum circuit configurations for a given set of requirements. The circuit is uniquely adapted to voltage sources with high regulation and represents the ultimate achievable, at the present time, in terms of minimum weight and maximum efficiency while using conventional circuit components. (A theoretical discussion is given in 5. 3).

Design information will be developed in terms of system parameters. The operation of the converter will then be demonstrated in conjunction with a hydrogen-air, fuel cell power source.

The individual sub-tasks associated with the "flyback" circuit development may be listed as:

1. Analytical evaluation and conceptual illustration of power circuit operation.
2. Calculation of major power circuit component values as a function of variable system parameters.
3. Calculation of system parameters for minimum circuit weight.
4. Powe r Circuit Design.
5. Design of transistor drive circuit.
6. Design of feedback control circuit.
7. Breadboard fabrication.
8. Breadboard evaluation.

5.2.3 High Frequency Switching Investigation

The high frequency switching investigation is directed toward increasing the operating frequencies of voltage converter circuits in order to reduce circuit weight without sacrificing efficiency.

Circuit performance will be studied with operating frequencies up to 100 kcps. Advanced circuit components such as powdered iron core transformers, ferrite core transformers, high speed switching power transistors and fast recovery diodes will be included in this task. Optimum operating frequencies will be established with respect to efficiency and weight, and feasibility hardware will be designed and constructed for evaluation.

The high frequency switching investigation is divided into those broad areas of study as follows:

1. Initial comprehensive examination

2. Component investigation

3. Circuit design and evaluation

The initial examination will consist of establishing the operation of an ideal inverter circuit. A typical circuit such as a push-pull inverter will be used as a reference in establishing modes of operation and design considerations, pertaining to increased operating frequencies. The initial examination will also define circuit component considerations with respect to broad areas of power loss.

The second area of investigation will be directed toward circuit component evaluation. Since increased frequency of operation generally results in higher electrical losses, a thorough examination must be made of:

a) solid state elements
b) inductive components
c) dielectric components
d) choice of material
e) configuration aspects

Losses for those basic components will be calculated as a function of frequency to provide design information with respect to selecting optimum component performance.

The third area of investigation consists of a circuit design and evaluation. The results of the first two areas of study will be used to select an optimum frequency based on weight and loss considerations.

A model breadboard will then be designed and constructed to demonstrate and evaluate the analytical results of the study.

5.2.4 AC Wave Shaping Techniques

It was readily apparent from the results of the previous study that the inductive and capacitive networks required for providing a sinusoidal output with less than 5% total harmonic content placed a severe penalty on the weight of the circuit. In addition, output voltage regulation by means of pulse width modulation results in inefficient component utilization since the net harmonic content of the output wave is a function of applied load which in turn influences the conduction interval causing a variable harmonic content dependent upon load conditions. Filter designs then are based on a "worst case" condition and are generally overdesigned for fractional loads.

Thus, the efforts of this task will be devoted to investigating the methods of reducing inverter output filtering requirements by use of direct AC wave-shaping techniques. The objectives of this task are as follows:

1. Establish methods of reducing inverter weight, and increasing efficiency through such techniques as multiple pulse width modulation and stepped wave modulation.

2. Establish design information showing weight, efficiency of these optimum circuits.

3. Demonstrate the results of the study by means of a representative inverter model.

5.2.5 Advanced Device Investigation

Although rapid advancements have been made in the current rating, voltage rating and power capabilities of semiconductors, there are still areas where improvements can be made to increase the overall efficiency of devices operating in a switching mode. Since the solid state switching device is the heart of any static converter circuit, it is planned to investigate devices from a standpoint of obtaining improved power transistors and to explore the utility of new devices such as tunnel diodes, light sensitive silicon controlled rectifiers (SCR) and gate turn-off silicon controlled rectifiers.

The major losses in power transistors operating in the switching mode are those associated with the turn-on time, the ohmic resistance during the conduction interval, and turn-off time. These factors are either directly or indirectly related to the voltage rating of transistors in such a manner that the stated losses tend to increase with increased voltage blocking capability. Since the past impetus in power transistor development has been directed toward increasing the voltage rating, a correspondingly lesser effort has been devoted to minimizing conduction and switching losses. This approach has been justified because at the higher operating voltages, and the relatively low switching frequencies associated with higher powers, the transistor losses tend to become negligible. However, at the lower voltage levels normally associated with present day unconventional sources, ohmic conduction losses become significant with respect to other circuit losses. Lower voltages also imply switching high currents which increases the severity of losses caused during the turn-on and turn-off interval.

The effort in this phase will be devoted to exploiting the lower voltage requirements of this study by trading off characteristics so as to minimize losses. A study of ratings and characteristics of importance to conversion circuits will result in establishing specifications for a power-transistor which is particularly suited for low voltage application.

5.2.6 Circuit Reliability and Protection

Because of the inherent nature of power conversion circuit operation, design techniques for increasing reliability must be considered. The switching of large currents and the resultant voltage transients represent a severe mode of operation which is prevalent even in the steady state condition. Reactive loading and step changes in loading compound the severity of operation. Design techniques and circuit functions must be incorporated to protect the circuit during fault conditions. Potentially critical circuit functions should be defined.

During this portion of the investigation, the objectives will be to:

1. Define the factors contributing to high circuit reliability.

2. Establish design techniques for increasing reliability of voltage conversion circuitry.

3. Establish techniques and methods of protecting circuits during fault conditions.

5.2.7 Advanced Circuit Concept Study

The achievement of low weight, highly efficient voltage conversion circuits requires optimum component utilization. In general, this requires use of a minimum number of power components with any given component serving more than one function. For example, the flyback circuit utilizes an inductor to perform both a voltage step up and a filtering function. In this manner, circuit weight is reduced and efficiency increased.

The purpose of the advanced circuit concept study is to determine optimum circuit design principles and to design voltage conversion circuits particularly suited for use with unconventional power sources. The study is a fundamental circuit investigation with the initial effort being devoted to a quantitative definition of the weight and efficiency characteristics of the optimum power components. These components include the transformers, inductors, capacitors, transistors plus heat sinks, and rectifiers plus heat sinks.

The second phase of the study will involve establishing optimum circuit design principles for, and design of DC-DC circuits. Emphasis will be given to use of a minimum number of power components by combination of circuit functions, and also to circuit arrangements which minimize the amount of power which must be handled by any given components. The procedure will involve a repeating process of circuit synthesis, evaluation, and new circuit synthesis using information learned.

The third phase of the study is the same as the second phase except that it is directed toward DC-AC circuits.

The results of the effort will be a definition of the optimum circuit design principles, a description of the optimum circuits resulting from the study, and data indicating weight and efficiency characteristics of these circuits.

5.3 Flyback Circuit Development

Contents

5.3.1 Summary

The "fly-back" power circuit and its associated time-ratio control (TRC) circuit for its power switch are discussed. Formulae for parameters and operation of the power circuit are presented as are formulae for one type of TRC circuit. This report treats the basic power circuit and the TRC circuits as separate entities since any of a variety of TRC circuits could be employed depending on the degree of sophistication required.

Results of tests for the power circuit indicate substantial agreement with performance predicted from theoretical considerations. This is to be expected because the circuit is simple - two capacitors, one reactor, switch and a diode.

Test results for the first TRC circuit indicated its region of operation was limited. Further investigation indicated an inherent limitation in this control circuit which made it inadequate for the immediate application.

Another TRC circuit is under development. The circuit is expected to operate from full load down to no load.

The design goal is a weight of 35 pounds per kilowatt for all components including control. Based on 84.5 watts maximum input and a converter efficiency of 90 percent the component weight should not exceed 2.66 pounds.

5.3.2 Converter Input Specifications

Input to the converter is the output of a fuel cell power source. The nature of present and projected fuel cell characteristics for this application makes necessary a converter which is designed to operate through a wide band of possible power and current levels. Figure 5.3-1 shows this operating band. It stretches from zero input (at 16 to 17 volts) to 84.5 watts input at 8 amps. The input ripple voltage caused by the operation of the converter circuit is to be limited to 10 percent (Peak-peak) of the average source voltage at 76 watts, 9.5 volts input, which is the most severe operating condition. Converter efficiency is to be at least 90 percent in the band above 15 watts.

5.3.3 Power Circuit

A. Introduction

Our problem at hand is not unlike that of a pumped-storage hydro-electric development. This hydro system pumps part of the stream to a higher elevation. Potential energy which is imparted to this water is obtained from the undiverted water in its descent to a lower elevation.

In our converter circuit part of the electrons from the source are raised to a higher potential for delivery to the load. The potential energy is obtained from the undiverted electron stream which is channeled to ground via the switch.

A reactor is an energy storage device and upon this principal the basic circuit concept is built. Electrical energy is handled most conveniently in batches or by cyclic operation. Control is achieved by ratioing the energizing and "kicking" intervals. For a given period, the voltage step-up is greater for a longer energizing interval. Thus, the output capacitor is "pumped" up to a specified output potential and held there by supplying just enough make-up energy for the load.

The basic power circuit is shown in Figure 5.3-2 with power transistor Q_1 for the static switching element. Figures 5.3-3, 4, 5, and 6 show the operating volts and amps at significant points in the circuit for full load conditions.

For light load conditions, the circuit may be designed to have either a continuous or discontinuous reactor current. A significant overall weight reduction is possible by designing a small reactor for discontinuous current even though this will require some weight to be added for filtering in the capacitor sections. Figures 5.3-7, 8, and 9 show the operating volts and amps in the circuit for the condition of light load.

B. Theoretical Analysis

Basic Equation

The flyback circuit performs conceptually to transfer energy from a low voltage bus to a high voltage bus. The circuit consists of a reactor L, and power switch Q_1 and a diode D. In practice, the source may require stiffening with capacitor C_1 and the output usually requires a smoothing capacitor C_2. Arrangement of these parameters is shown in Figure 5.3-10.

Circuit analysis is oriented toward reactor functions. Initially let it be assumed that source voltage E_s and load voltage E_ℓ are constant, and that the circuit is lossless. During the energizing interval, Δt_1, when the reactor is shorted across the source through switch Q_1:

$$L \frac{(\Delta i_L)_1}{\Delta t_1} = E_s$$

$$(5.3\text{-}1) \quad \text{or} \quad (\Delta i_L)_1 = \frac{E_s}{L} \Delta t_1$$

During the "kicking" interval, Δt_2:

$$L \frac{(\Delta i_L)_2}{\Delta t_2} = E_s - E_\ell$$

$$(5.3\text{-}2) \quad \text{or} \quad (\Delta i_L)_2 = -\frac{(E_\ell - E_s)}{L} \Delta t_2$$

Now $(\Delta i_L)_1 = -(\Delta i_L)_2$

Thus from equations 5.3-1 and 5.3-2:

$$(5.3\text{-}3) \qquad \frac{E_s}{L} \Delta t_1 = \frac{(E_\ell - E_s)}{L} \Delta t_2$$

$$(5.3\text{-}4) \text{ or } \quad E_s \left(1 + \frac{\Delta t_1}{\Delta t_2}\right) = E_\ell$$

Since $\Delta t_2 = T - \Delta t_1$, where T is the period, we can substitute for Δt_2 in 5.3-4:

$$(5.3\text{-}5) \qquad \frac{E_\ell}{E_s} = \left(1 + \frac{\Delta t_1}{T - \Delta t_1}\right)$$

Solving for Δt_1:

$$(5.3\text{-}6) \qquad \Delta t_1 = T\left(1 - \frac{E_s}{E_\ell}\right)$$

Since $\Delta t_2 = T - \Delta t_1$, then from 5.3-6:

$$(5.3\text{-}7) \qquad \Delta t_2 = T \frac{E_s}{E_\ell}$$

The reactor current varies in a sawtooth manner as shown in Figure 5.3-4. It will be convenient for future calculations to define the magnitude of the peak to peak sawtooth ripple as a fraction f of the source current, i_s.

$$(5.3\text{-}8) \qquad \Delta i_L = f i_s$$

Substituting Δi_L from equation 5.3-8 and Δt_2 from equation 5.3-7 into 5.3-2 yields:

$$(5.3\text{-}9) \qquad L \frac{f i_s}{T \frac{E_s}{E_\ell}} = E_\ell - E_s$$

Solving for f:

$$(5.3\text{-}10) \qquad f = \frac{(E_\ell - E_s) T E_s}{L i_s E_\ell}$$

Obviously, the ripple fraction is largest when reactance L and source current i_s are least.

When the load is made to decrease, the trough of the sawtooth will eventually reach zero. For this light load operating condition, f is 2 since the maximum reactor current at the peak of the sawtooth is twice source current i_s. If the load is further decreased, the reactor current rests at zero for a short interval, Δt_{2b} as shown in Figure 5.3-8.

Source Capacitor - C_1

The capacitor C_1 in Figure 5.3-10 cushions the source from the effects of abruptly switching a finite inductance in the circuit. It has been assumed the residual ripple across C_1 will have second order effects on circuit operation. Now the size of C_1 will be determined which will meet the specification of 10 percent voltage ripple at the source.

Referring to Figure 5.3-4, the voltage change on capacitor C_1 is:

$$(5.3\text{-}11) \qquad \Delta V_{C1} = \frac{1}{C_1} \int_{0}^{\frac{\Delta t_1}{2} + \frac{\Delta t_2}{2}} i_{C1}\, dt$$

Now:

$$(5.3\text{-}12) \qquad i_{C_1\ avg.} = \frac{\Delta i_L}{4}$$

and:

$$(5.3\text{-}13) \qquad \frac{\Delta t_1}{2} + \frac{\Delta t_2}{2} = \frac{T}{2}$$

Thus from equation 5.3-11:

$$(5.3\text{-}14) \qquad \Delta V_{C1} = \frac{1}{C_1} \quad \frac{\Delta i_L}{4} \quad x \quad \frac{T}{2}$$

Dividing ΔV_{C1} by E'_s (uncorrected source voltage) gives the per unit ripple as:

$$(5.3\text{-}15) \qquad \left(\frac{\Delta V_{C1}}{E'_s}\right) = \frac{T \Delta i_L}{8 C_1 E'_s}$$

Substituting Δi_L from equation 5.3-8 in 5.3-15 gives:

$$(5.3\text{-}16) \qquad \left(\frac{\Delta V_{C1}}{E'_s}\right) = \frac{T(f\, i_s)}{8 C_1 E'_s}$$

Solving for C_1:

$$(5.3\text{-}17) \qquad C_1 = \frac{T f i_s}{8E'_s\left(\frac{\Delta V_{C1}}{E'_s}\right)}$$

Factor $\left(\frac{\Delta V_{C1}}{E'_s}\right)$ is the allowable ripple peak to peak in the source voltage.

The value of C_1 is equation 5.3-17 is usually largest for full load conditions and the value of f should be obtained from equation 5.3-10 for full load conditions. If the application involves a small step-up ratio such as about 1 at no load, the minimum value of C_1 will probably be determined for a load condition other than full load. It is suggested that a curve of C_1 be determined over the load range in order to find the correct value of C_1.

Output Capacitor - C_2

A capacitor is required to supply energy to the load during the interval when no energy is being supplied by the reactor. Figure 5.3-5 illustrates the capacitor current i_{C2} and voltage ripple. Obviously, the value of C_2 is determined by full load conditions when the capacitor supplies load current i_ℓ during the energizing interval Δt_1.

The change in capacitor voltage is given by:

$$(5.3\text{-}18) \qquad \Delta V_{C2} = \frac{1}{C_2} \; i_\ell \; \Delta t_1$$

Dividing by load voltage E'_ℓ gives the per unit ripple voltage on a peak to peak basis:

$$(5.3\text{-}19) \qquad \left(\frac{\Delta V_{C2}}{E'_\ell}\right) = \frac{1}{C_2} \; \frac{i_\ell}{E'_\ell} \; \Delta t_1$$

Solving equation 5.3-19 for C_2:

$$(5.3\text{-}20) \qquad C_2 = \frac{\Delta t_1 \; i_\ell}{E'_\ell\left(\frac{\Delta V_{C2}}{E'_\ell}\right)}$$

where $\frac{\Delta V_{C2}}{E'_{\ell}}$ is the allowable ripple peak to peak in the output voltage.

Reactor - L

The derivation of reactance L involves new per unit parameters J and K as defined in Figure 5.3-11. In this diagram the areas "A" and "B" represent coulomb flow into and out of capacitor C_2. Hence, they must be equal. Also areas "C" and "D" which represent coulomb flow out of and into capacitor C_1 must be equal.

Setting areas "C" and "D" equal establishes a key equation for Δi_L which permits showing that areas "A" and "B" are equal and allows solving for inductance L.

Thus:

$$\text{Area "C"} = 1/2 \text{ width x height}$$

$$= 1/2 \left[T J \left(1 - \frac{i_s}{\Delta i_L} \right) (\Delta i_L - i_s) \right]$$

$$= \frac{T J}{2} \left[\Delta i_L - i_s - i_s + \frac{i_s^2}{\Delta i_L} \right] \qquad (5.3\text{-}21)$$

and:

$$\text{Area "D"} = T i_s \left[1 - J \left(1 - \frac{i_s}{2\Delta i_L} \right) \right]$$

$$= \frac{T J}{2} \left[\frac{2i_s}{J} - 2i_s + \frac{i_s^2}{\Delta i_L} \right] \qquad (5.3\text{-}22)$$

In order for Area "C" to equal Area "D", it is necessary that:

$$\Delta i_L = \frac{2i_s}{J} \qquad (5.3\text{-}23)$$

Now equation 5.3-23 can be used to show areas "A" and "B" are equal.

Thus:

$$\text{Area "A"} = 1/2 \left[T(J - K) \left(1 - \frac{i_\ell}{\Delta i_L} \right) \right] \left[(\Delta i_L - i_\ell) \right]$$

$$= i_\ell T \left(1 - \frac{i_\ell}{\Delta i_L} \right)^2 \qquad (5.3\text{-}24)$$

and:

$$\text{Area "B"} = i_\ell T \left[1 - (J - K) \left(1 - \frac{i_\ell}{2\Delta i_\ell} \right) \right]$$

$$\text{but } K = J \left(1 - \frac{i_\ell}{J\Delta i_L} \right) = \left[J - \frac{2i_\ell}{\Delta i_L} \right] \qquad (5.3\text{-}25)$$

Thus:

$$\text{Area "B"} = i_\ell T \left\{ 1 - \left[J - \left(J - \frac{2i_\ell}{\Delta i_L} \right) \right] \left(1 - \frac{i_\ell}{2\Delta i_L} \right) \right\}$$

$$= i_\ell T \left[1 + \frac{2i_\ell}{\Delta i_L} - \left(\frac{i_\ell}{\Delta i_L} \right)^2 \right]$$

$$= i_\ell T \left(1 - \frac{i_\ell}{\Delta i_L} \right)^2 \qquad (5.3\text{-}26)$$

which is the same area as area "A" in equation 5.3-24.

Note that the rise and fall in reactor current i_L as given by equation 5.3-23 is 1/J times the value it would have if the reactor were designed for continuous current at light load. Now the inductance L may be determined:

During the energizing interval Δt_1:

$$L \frac{\Delta i_L}{\Delta t_1} = E_s \qquad (5.3\text{-}27)$$

From equation 5.3-23:

$$(5.3\text{-}23) \qquad \Delta i_L = \frac{2i_s}{J}$$

Also, the energizing interval Δt_1 in Figure 5.3-11 is J times the value it would have had if the reactor had been designed for continuous current:

$$(5.3\text{-}28) \qquad \Delta t_1 = J\,T\left(1 - \frac{E_s}{E\ell}\right)$$

Substituting for Δi_L and Δt_1 in equation 5.3-27 gives:

$$(5.3\text{-}29) \qquad \frac{L\left(\frac{2i_s}{J}\right)}{JT\left(1 - \frac{E_s}{E\ell}\right)} = E_s$$

Solving for L:

$$(5.3\text{-}30) \qquad L = \frac{E_s J^2 T\left(1 - \frac{E_s}{E\ell}\right)}{2i_s}$$

Reactor Design

The following is a summary of the equations and constants required in the reactor design. Both a single "C" core-double coil, and a double "C" core-single coil reactor are considered.

Single "C" Core - Double Coil

$$(5.3\text{-}31) \qquad \text{(a)} \quad DEFG = (1/2I_m^2\,L)\left(\frac{200 \times 10^6}{V_w \times S.F. \times B_{m_{fe}} J_m}\right) \text{ inches}^4.$$

(b) MLT = $2(D + E) + \frac{\pi}{2}F$ (mean length of turn) inches.

(c) Xsec. cu. = $V_w \times F \times G$ (cross section of copper in window)

(d) Vol. cu. = MLT x Xsec. cu. (volume copper) inches^3.

(e) Wt. cu. = ρ_c x Vol. cu. (weight copper) pounds.

(f) Watts cu. = J_{rms}^2 x σ x Vol. cu. (loss in copper) watts.

(g) $$N = \frac{J_m V_w F \times G}{I_m}$$ total turns

(h) $$g = \frac{\mu_o J_m V_w \times F \times G}{2 B_{m_{fe}} \times S.F.}$$ inches each gap

where: D, E, F and G are core dimensions

V_w is window utilization factor

ρ_c is weight density of copper (.34 lb/in^3)

σ is electrical resistivity of copper (ohm-inches)

J_{rms} is RMS current density in copper

J_m is maximum current density in copper

$B_{m_{fe}}$ is maximum flux density in iron (line/in^2)

S.F. is iron stacking factor

N is total turns in <u>two</u> coils

g is thickness of each air gap (inches)

μ_o is permeability of air (3.19)

Xsec. cu. is cross section of copper

Current densities in the reactor are based on the source current (i_s):

(i) $$I_m = i_s \left(1 + \frac{f}{2}\right)$$

(j) $$I_{rms} = i_s \times \sqrt{1 + \frac{1}{3}\left(\frac{f}{2}\right)^2}$$

(5.3-10) where $f = \dfrac{(E_\ell = E_s)\ T\ E_s}{L i_s E_\ell}$

Some practical values for the factors in these equations are:

V_w = .35 to .50

ρ_c = .34

σ = $.734 \times 10^{-6}$ at 40°C

S.F. = .90 for 4 mil tape

$B_{m_{fe}}$ = 96,750 lines per sq. in.

J_m = 1000 amps per sq. in.

Copper losses can be kept low if the "C" core window area F x G is kept small in relation to the gross area D x E. When it comes to selecting a core on the basis of calculated DEFG a few trials will indicate the best core choice. Of course, DEFG of the actual core will probably be slightly different than the calculated core. Current density, flux density or some other factor must be revised accordingly. The number of turns N will more likely than not come out a fraction of a turn. Adjustment for this must be made in the calculations. The best cores seem to be those with D approximately equal to E. Allowance in the design should be made for some flux fringing at the gap.

Double "C" Core - Single Coil (Figure 5.3-13)

(5.3-32) (a) $DEFG = (1/2\ I_m^{\,2}\ L)\left(\dfrac{100 \times 10^6}{V_w\ S.F.\ B_{m_{fe}}\ J_m}\right)$ each core

(b) $MLT = 2(D + 2E) + \pi F$

(c) Xsec. cu. = $V_w \times F \times G$

(d) Vol. cu. = MLT x Xsec. cu.

(e) Wt. cu. = ρ_c x Vol. cu.

(f) Watts cu. = $J_{rms}^{\,2}\ \sigma$ x Vol. cu.

$$(g) \quad N = \frac{J_m V_w F \times G}{I_m}$$

$$(h) \quad g = \frac{\mu_o J_m V_w F \times G}{2 B_{m_{fe}} \times S.F.} \text{ each gap}$$

The same general comments as well as the nomenclature apply in these formulae as they did for the single "C" core - double coil design.

C. Design Calculations

Reactance, L, was derived in terms of source voltage E_s and load voltage E_ℓ. Of course, the net voltage applied to the inductor is less than the actual source voltage. Calculations should take into consideration the various voltage drops and rises in the circuit. For example, E_s in the formulae is taken to mean the net circuit voltage, i.e. source voltage less IR drops in reactor less forward drop through the switch. E_ℓ is taken to mean load voltage plus IR drop in C_2 plus forward drop in the diode. These corrections are small but significant. Corrected values for net E_s and E_ℓ are not exact but more precise calculations could seldom be justified.

Circuit Calculations

At 76 watts input (9.5 volts and 8 amps):

(5.3-33) $E_s = E'_s$ - IR drop (L) - Forward Drop (Q_1) - all other

$= 9.5 - .10 - .15 - .10$

$= 9.15$ volts

(5.3-34) $E_\ell = E'_\ell$ + diode drop + capacitor (C_2) IR drop

$= 28 + .55 + .10$

$= 28.65$ v

At 5 watts input (14.8 volts):

(5.3-35) $E_s = 14.8 - .10 - .10 - 0$

$= 14.60$

(5.3-36) $E_\ell = 28 + .4 + 0 = 28.4$

Reactor Calculations

Inductance L is determined by light load conditions. Arbitrarily use J = .5 and T = 667 micro-seconds.

$$(5.3\text{-}30) \quad L = \frac{E_s J^2 T \left(1 - \frac{E_s}{E_\ell}\right)}{2 i_s} \text{ henries}$$

Since $i_s = \frac{P_{in}}{E_s}$ amps:

$$(5.3\text{-}37) \quad L = \frac{E_s^2 J^2 T \left(1 - \frac{E_s}{E_\ell}\right)}{2 \times P_{in}} \text{ henries}$$

At light load:

$$E_s = 14.6 \text{ v}$$

$$E_\ell = 28.4 \text{ v}$$

$$P_{in} = 5 \text{ w}$$

$$J = .5$$

$$T = 667 \times 10^{-6}$$

Thus:

$$L = \frac{14.6^2 \times .5^2 \times 667 \times 10^{-6} \times \left(1 - \frac{14.6}{28.4}\right)}{2 \times 5}$$

$$= 1.73 \times 10^{-3} \text{ henries}$$

The maximum current, I_m, is determined by the 76 watt input condition when:

$$E_\ell = 28.65$$

$$E_s = 9.15$$

$$P_{in} = 76 \text{ w}$$

$$(5.3\text{-}10) \qquad f = \frac{(E_\ell - E_s)\ T\ E_s}{L\ i_s\ E_\ell}$$

Since $i_s = \frac{P_{in}}{E_s}$ amps:

$$(5.3\text{-}39) \qquad f = \frac{(E_\ell - E_s)\ T\ E_s^{\,2}}{L \times P_{in} \times E_\ell}$$

Thus at 76 watts, f is:

$$(5.3\text{-}40) \qquad f_{76w} = \frac{(28.65 - 9.15) \times 667 \times 10^{-6} \times 9.15^2}{1.73 \times 10^{-3} \times 76 \times 28.65}$$

$$= .298$$

$$(5.3\text{-}31) \quad (i) \qquad I_m = i_s \left(1 + \frac{f}{2}\right)$$

$$= 8 \left(1 + \frac{.298}{2}\right)$$

$$(5.3\text{-}41) \qquad = 9.18 \text{ amps}$$

$$(j) \qquad I_{rms} = i_s \sqrt{1 + \frac{1}{3}\left(\frac{f}{2}\right)^2}$$

$$= 8\sqrt{1 + \frac{1}{3}\left(\frac{.298}{2}\right)^2}$$

$$(5.3\text{-}42) \qquad = 8.03 \text{ amperes}$$

For the single "C" core - double coil:

$$(5.3\text{-}31) \quad (a) \quad DEFG = (1/2\, I_m^{\,2}\, L)\left(\frac{200 \times 10^{-6}}{V_w \times S.F. \times B_{m_{fe}} \times J_m}\right)$$

Let $V_w = .35$, $S.F. = .9$ $B_{m_{fe}} = 15$KG, $J_m = 10000$:

$$(5.3\text{-}43) \quad (a) \quad DEFG = (1/2 \times 9.18^2 \times 1.73 \times 10^{-3}) \left(\frac{200 \times 10^{-6}}{.35 \times .9 \times 96,750 \times 1000}\right)$$

$$= .478$$

For an Arnold Core A Z - 8:

wt. = .89 pounds

DEFG = .616

Therefore $J_m = \frac{.478}{.616} \times 1000 = 776$, and $J_{rms} = \frac{8.03}{9.18} \times 776 = 680.$

(b) $MLT = 2(D + E) + \frac{\pi F}{2} = 2\left(1 + \frac{9}{16}\right) + \frac{\pi}{2} \times \frac{5}{8} = 4.11$

(c) X-sec. cu. $= V_w \times F \times G = .35 \times 1.09 = .381$

(d) Vol. cu. = MLT x X - sec. cu. 1 4.11 x .381 = ..157

(e) Wt. cu. $= \rho_c \times$ Vol. cu. = .34 x 1.57 1= .533 pounds

Iron and Copper wt. = .89 + .533 = 1.42 pounds

(f) Watts cu. $= J_{rms}^{\,2} \times \sigma \times$ Vol. cu.

$= 680^2 \times .734 \times 10^{-6} \times 1.57 = .53$ watts

$$(g) \quad N = \frac{J_m V_w (F \times G)}{I_m}$$

$$= \frac{776 \times .35 \times 1.09}{9.18} = 32.2 \text{ turns}$$

or 32 turns

$$(h) \quad g = \frac{\mu_o J_m V_w \times F \times G}{2B_{m_{fe}} \quad S.F.}$$

$$= \frac{3.19 \times 776 \times .35 \times 1.09}{2 \times 96,750 \times .9} = .00545 \text{ inches}$$

Strand cross-section $= \frac{I_m}{J_m} = \frac{9.18}{776} = 11,820$ sq. mils

Input Capacitor C_1 Calculations

$$(5.3\text{-}17) \quad C_1 = \frac{R f i_s}{8 E'_s \left(\frac{\Delta V_{C1}}{E'_s}\right)}$$

At 76 watts;

$E'_s = 9.5$ volts

$I_s = 8$ amps

$f_{76w} = .298$

Let $\frac{\Delta V_{C1}}{E'_s} = .10$

Substituting in (5.3-17)

$$(5.3\text{-}44) \quad C_1 = \frac{667 \times 10^{-6} \times .298 \times 8}{8 \times 9.5 \times .10}$$

$C_1 = 209$ micro-farad

Use 1 unit 29F488 rated 350 mfd - 25 volts - Polar - Case D-3, wt. .03 pounds.

Acceptable ripple = .881 volts from capacitor specs.

$$\text{Actual RMS ripple} = \frac{.10 \times 9.5}{\sqrt{3}} \times \frac{209}{350} = .348 \text{ volts.}$$

Resistance from capacitor specs = .114 ohms

$$(5.3\text{-}45) \quad I_{C1} = \frac{V_{C1}}{X_{C1}} = \frac{.348}{\frac{1}{2\pi f C_1}} \text{ rms}$$

$$= .348 \times 9420 \times 350 \times 10^{-6} = 1.15 \text{ a}$$

$$(5.3\text{-}46) \quad I_{C1}^{\ 2} R_{C1} = 1.15^2 \times .114 = .151 \text{ watts}$$

Output Capacitor C_2 Calculations

$$(5.3\text{-}20) \quad C_2 = \frac{\Delta t_1 \, i_\ell}{E'_\ell \left(\frac{V_{C2}}{E'_\ell} \right)}$$

At 76 watts:

$$E'_\ell = 28 \text{ v}$$

$$E_\ell = 28.65 \text{ v}$$

$$E_s = 9.15 \text{ v}$$

$$\Delta t_1 = T \left(1 - \frac{E_s}{E_\ell} \right) = 454 \times 10^{-6}$$

Let:

$$\left(\frac{\Delta V_{C2}}{E'_\ell} \right) = .05$$

$$\eta_c = .90$$

(5.3-47) $$i_\ell = \frac{P_{in} \times \eta_c}{E'_\ell} = \frac{76 \times .9}{28} = 2.44$$

(5.3-48) $$C_2 = \frac{454 \times 10^{-6} \times 2.44}{28 \times .05} = 791 \text{ mfd.}$$

Use 2 units 29F1099 polar etched 1100 mfd each; case no. 10, wt. .20 pounds each.

Acceptable ripple from specs. = .59 volts rms

Actual RMS ripple = $\frac{.05 \times 28}{\sqrt{3}} \times \frac{791}{2 \times 1100} = .306$ volts

Resistance from capacitor specs. = .0364 ohms each.

(5.3-49) $$I_{C2} = \frac{V_{C2}}{X_{C2}} = .306 \times 9420 \times 2200 \times 10^{-6} = 6.34 \text{ amps.}$$

(5.3-50) $$I_{C2}^2 R_{C2} = 6.34^2 \times \frac{.0364}{2} = .74 \text{ watts}$$

Diode Calculations

(5.3-51) $$(i_{D\ avg})_2 = i_s = 8a \text{ at } 76 \text{ watts input}$$

(5.3-52) $$\Delta t_2 = T \frac{E_s}{E_\ell} = 667 \times 10^{-6} \times \frac{9.15}{28.65} = 213 \times 10^{-6}$$

forward drop = .55 volts avg.

$$T = 667 \times 10^{-6}$$

(5.3-53) $$\text{Avg. watts} = (i_{D\ avg})_2 \times \text{forward drop} \times \frac{\Delta t_2}{T}$$

$$= 8 \times .55 \times \frac{213 \times 10^{-6}}{667 \times 10^{-6}} = 1.57 \text{ watts}$$

Summary of Calculations for Major Components Except Switch and Control

		wt. lbs.	Losses-Watts
Reactor L	1.57 mh	1.42	.65 + core loss
Input Capacitor C_1	350 mfd	.03	.12
Output Capacitor C_2	2200 mfd	.40	.74
Diode D		.07	1.57
	TOTAL	1.92 lbs.	3.11 watts

5.3.4 Some Other Power Circuits

The reactor-switch configuration may be varied when there is an advantage to do so. This is possible because the energy which is stored in the air gap of a reactor can be put in with one winding and can be taken out with another. Three variations are shown in Figure 5. 3-14.

Tapped Reactor

Figure 5. 3-14a shows a 90 turn reactor tapped at 36 turns - the following analysis applies:

$$(5.3\text{-}54) \qquad \frac{L_1(\Delta i_L)_1}{\Delta t_1} = E_s$$

Rearranging:

$$(5.3\text{-}55) \qquad (\Delta i_L)_1 = \frac{E_s}{L_1}\,\Delta t_1$$

and

$$(5.3\text{-}56) \qquad \frac{L_2\,(\Delta i_L)_2}{\Delta t_2} = -(E_\ell - E_s)$$

Rearranging:

$$(5.3\text{-}57) \qquad (\Delta i_L)_2 = - \frac{(E_\ell - E_s)}{L_2} \Delta t_2$$

Since the flux density change in the gap is the same up and down, the change in ampere-turns must be equal:

$$(5.3\text{-}58) \qquad (\Delta i_L)_1 = - (\Delta i_L)_2 \times \sqrt{\frac{L_2}{L_1}}$$

$$(5.3\text{-}59) \qquad \text{where:} \quad \sqrt{\frac{L_2}{L_1}} = \frac{N_1 + N_2}{N_1}$$

From equations 5.3-55 through 5.3-58:

$$(5.3\text{-}60) \qquad \frac{E_s \Delta t_1}{L_1} = \frac{(E_\ell - E_s)}{L_2} \Delta t_2 \sqrt{\frac{L_2}{L_1}}$$

Multiplying equation 5.3-61 by $\sqrt{L_1}$ there results:

$$(5.3\text{-}61) \qquad \frac{E_s \Delta t_1}{\sqrt{L_1}} = \frac{(E_\ell - E_s)}{\sqrt{L_2}} \Delta t_2$$

$$(5.3\text{-}62) \qquad = \frac{(E_\ell - E_s)}{\sqrt{L_2}} (T - \Delta t_1)$$

Factoring and transposing:

$$(5.3\text{-}63) \qquad \Delta t_1 \left(\frac{E_s}{\sqrt{L_1}} + \frac{(E_\ell - E_s)}{\sqrt{L_2}} \right) = T \frac{(E_\ell - E_s)}{\sqrt{L_2}}$$

Solving:

$$(5.3\text{-}64)\quad \frac{\Delta t_1}{T} = \frac{\dfrac{(E_\ell - E_s)}{\sqrt{L_2}}}{\dfrac{E_s}{\sqrt{L_1}} + \dfrac{(E_\ell - E_s)}{\sqrt{L_2}}} = \frac{1}{1 + \sqrt{\dfrac{L_2}{L_1}}\ \dfrac{E_s}{(E_\ell - E_s)}}$$

$$(5.3\text{-}59)\quad \text{where: } \sqrt{\frac{L_2}{L_1}} = \frac{N_1 + N_2}{N_1}$$

At full load E_ℓ and E_s are fixed but we can adjust $\frac{\Delta t_1}{T}$ and $\sqrt{\frac{L_2}{L_1}}$ to satisfy equation 5.3-64. The significance of this is that the operating range of the TRC circuit can be partially controlled by reactor turns ratio.

Source current, i_s, is given by:

$$(5.3\text{-}60)\quad i_s = i_{L\ \text{avg.}}$$

$$(5.3\text{-}61)\quad = \frac{(i_L)_1\ \Delta t_1 + (i_L)_2\ \Delta t_2}{T}$$

Now:

$$(5.3\text{-}62)\quad (i_L)_1 = \sqrt{\frac{L_2}{L_1}}\ (i_L)_2$$

and:

$$(5.3\text{-}63)\quad (i_L)_2 = i_\ell\ \frac{T}{\Delta t_2}$$

From equations 5.3-62 through 5-3-63:

$$(5.3\text{-}64) \qquad i_s = \frac{\sqrt{\frac{L_2}{L_1}}\, i_\ell \frac{T}{\Delta t_2} \Delta t_1 + i_\ell \frac{T}{\Delta t_2} \times \Delta t_2}{T}$$

$$(5.3\text{-}65) \qquad i_s = \left(\sqrt{\frac{L_2}{L_1}} \frac{\Delta t_1}{\Delta t_2} + 1 \right) i_\ell$$

A reactor was built with the following design: $N_1 = 36T$ with $L_1 = 1.5$ mh
$N_2 = 54T$

The following test results were obtained:

$$E'_s = 9.5 \text{ v}, 5.28 \text{ a}$$
$$E_i = 27.9 \text{ v}, 1.25 \text{ a}$$
$$\frac{\Delta t_1}{T} \simeq 45 \text{ percent}$$

These results indicate the above analysis is substantially correct.

Although this circuit could be used for the present application it has some drawbacks. First, the reactor must be about 50 percent larger to avoid core saturation and to reduce I^2R loss in the reactor. Secondly, the power transistor must handle greater current which will result in greater switching losses.

Reactor with Isolated Secondary

Figure 5.3-14b shows the same reactor in another arrangement. This circuit may have some merit when isolation is important. Despite its relatively larger size it could be expected to perform better than a transformer-choke circuit.

Reactor with Separate Winding

Figure 5.3-14c shows another configuration which was tested. It performed as expected. This circuit is probably of academic value only since any advantage it may have is not obvious.

5.3.5 Control Circuit Number 1

A. Introduction

The complete flyback circuit employing control circuit number 1 is shown schematically in Figure 5.3-15. When power transistor Q_1 is turned on, a saturable current transformer (SCT) has its primary in series with a current source. The current transformer burden is substantially the diode drop of the transistor base-to-emitter voltage. The amount of reset on the B-H loop is a function of two factors: (1) the voltage applied to the reset winding and (2) the duration of this applied voltage. The following analysis summarizes the control circuit design.

B. Control Circuit Design

Figure 5.3-16 shows a simplified schematic diagram of the control circuit. A Delco 2N1523 power transistor was selected for the switch because of its low forward drop and a high current gain. A base drive of .75 amps was selected for an 8 amp load. The diode drop in the base is about 0.5 volts for .75 amps base current.

Equating ampere-turns in the SCT:

$$N_B i_B = N_E \left(i_E - \frac{H \times \ell}{N_E} \right) \qquad (5.3\text{-}66)$$

where H is reset ampere-turns per inch

ℓ is length of toroidal SCT core

and the other factors are defined in Figure 5.3-16

Rearranging equation 5.3-66:

$$N_B i_B = N_E i_E - (H \times \ell) \qquad (5.3\text{-}67)$$

But:

$$N_B = \frac{V_B}{\frac{\Delta \phi}{\Delta t_{1\ max}}} \times 10^{-8} \qquad (5.3\text{-}68)$$

From equations 5.3-67 and 5.3-68:

$$(5.3\text{-}69)\quad \frac{V_B}{\frac{\Delta\phi}{\Delta t_{1\ max}} \times 10^{-8}}\ i_B = N_E i_E - H \times \ell$$

Solving for N_E:

$$(5.3\text{-}70)\quad N_E = \frac{V_B i_B}{\frac{\Delta\phi}{\Delta t_{1\ max}} i_E \times 10^{-8}} + \frac{H\ell}{i_E}$$

or:

$$(5.3\text{-}71)\quad N_E = \frac{V_B i_B}{\frac{A_c \times 2B_m i_E}{1.25\,\Delta t_1} \times 10^{-8}} + \frac{H\ell}{i_E}$$

where: A_c is cross section of core (net)

B_m is maximum flux density in core

1.25 is flux saturation safety factor

H is coercive force in core

ℓ is length of magnetic circuit

For Magnetic-Metals Core No. 51002-1D:

$A_c = \frac{.081}{6.45} = .01257$ in.^{2}

$H = .15 \times 2.02 = .30$ NI/in.

$\ell = 6.13/2.54 = 2.42$ in.

$V_B = 0.50$ v

$i_B = .75$ a

$i_E = 8$ a

$B_m = 6,000 \times 6.45 = 38,700$ lines/in.^{2}

$\Delta t_{1\ max} = .451 \times 10^{-3}$ at 75 watts input

For the emitter winding:

$$(5.3\text{-}72) \quad N_E = \frac{.5 \times .75}{\frac{.01257 \times 2 \times 38,700 \times 8 \times 10^{-8}}{1.25 \times .454 \times 10^{-3}}} + \frac{.30 \times 2.42 \times .75}{8}$$

$$= 2.75 + .07 = 2.82 \text{ turns}$$

$$\text{Use} \quad N_E = 3 \text{ turns}$$

For the base winding:

$$(5.3\text{-}66) \quad N_B i_B = N_E \left(i_E - \frac{H \times \ell}{N_E} \right)$$

$$(5.3\text{-}73) \quad N_B \times .75 = 3 \left(8 - \frac{.30 \times 2.42}{3} \right)$$

Solving for N_B:

$$(5.3\text{-}74) \quad N_B = 3 \left(\frac{8 - .25}{.75} \right) = 31 \text{ turns}$$

In order to keep the reset winding current low, 100 turns was arbitrarily chosen:

$$N_B = 100 \text{ turns}$$

$$(5.3\text{-}75) \quad i_R = \frac{H \times \ell}{N_R}$$

$$(5.3\text{-}76) \quad i_R = \frac{.3 \times 2.42}{100}$$

$$= .0075 \text{ amps}$$

Let the current density in the SCT be about 1000 amps per sq. in. Then the following wire sizes become:

Winding	Turns	Wire
emitter	3	4/.0508 HF
base	31	1/.032 HF
reset	100	1/.005 HF

Summary of Switch and Control Losses

		Wt. Lbs.	Losses-Watts
Q_1	Base Drive	.07	.38
Q_1	Saturation Resistance	-	.50
Q_1	Switching Losses	-	3.26
SCT	Transformer	.20	.10
	All other	.10	.25
		.37 lbs.	4.49 watts

C. Test Results of Control Circuit No. 1

Control Circuit No. 1 failed to perform as conceived. As long as the voltage step-up required was such that the power transistor (Q_1) conduction interval was less than 45 percent of the period, the circuit behaviour was as anticipated. However, any attempt to increase the conduction interval beyond 45 percent of the period caused the circuit to operate in a bi-stable mode with alternate short and long conduction intervals.

This bi-stable phenomenon is characterized by its independence of frequency, core cross section, base drive turns and current being carried. Delta Max which was also tried exhibited the same phenomenon, but it entered the bi-stable mode more abruptly, the transistor was more difficult to turn "on" and the SCT required more reset ampere-turns.

With about 1.2 ohms in the base drive circuit the stable range can be extended from 45 percent up to about 55 percent. With resistance in the base drive circuit this upper limit became current sensitive.

If the reset is adjusted for a bi-stable mode and the power is turned on, the circuit seemed to operate properly for about the first 500 cycles before going into the bi-stable mode.

The "on" time Δt_1 in the calculations is based on instantaneous switching of voltage and current. Actually, the voltage is switched in a few micro-seconds while the current change in this circuit takes about 35 micro-seconds and appears to be about linear. Energy wasted in switching should properly be factored into all calculations. In evaluating control circuit no. 1 initial emphasis was placed on imparting functional integrity to the circuit rather than improving its switching performance. A design goal of 90 percent converter efficiency allows a switching loss of 3.26 watts. In order to realize this switching loss, the combined turn-"on" and turn-"off" times should not exceed about 17 micro-seconds at 1500 cps or 25 micro-seconds at 1000 cps.

Although this control circuit was disappointingly unstable for the present application, it can be used very effectively when the fuel cell is designed for a no-load voltage of about 28 volts. Its simplicity has merit and the control circuit should not be overlooked when such an application arises.

The following paragraphs explain the reasons for the unsatisfactory behaviour of control circuit no. 1 and give its inherent limitations.

D. Theory of Operation

The essentials of control circuit no. 1 are shown in Figure 5.3-17. This circuit steps up a source voltage E_s, such as that of a fuel cell, to a higher output voltage (E_O). The output voltage E_O is controlled by current I_C in a control winding that is insulated from the output and power source. The circuit as shown is unstable when $E_O \geq 2 E_S$. This limitation is overcome by the use of control circuit no. 2 described in section 5.3.6. The operation of the power portion of the circuit (Figure 5.3-17) involving L_F, D_F, C_F and the function of Q_1 is described in the previous paragraphs. This part presents the operation of control circuit no. 1 and shows the reason for the instability experienced.

The step down circuit of Figure 5.3-18 is used for describing the operation and problems. The operation of Q_1, ST_1 and the trigger of Figure 5.3-18 is similar to the circuit of Figure 5.3-17. The only difference in the control circuits of Figure 5.3-17 and 5.3-18 is $E_O > E_S$ in Figure 5.3-17, and $E_O < E_S$ in Figure 5.3-18. Both circuits have many applications for power conversion, and it is appropriate that this description apply to both. It is easier to illustrate the operation and problems of the control circuit in Figure 5.3-18 than in Figure 5.3-17. In Figure 5.3-18 the output voltage E_O is proportional to the amplitude of the flux change $\Delta\phi_R$ during reset. This permits a direct relation between E_O and $\Delta\phi_R$ which makes it easier to discuss the operation of this circuit.

The operation of control circuit of Figure 5.3-18 is illustrated by an idealized flux density-magnetomotive force curve (B-H) with related points to a transfer curve (E_O vs. I_C) as shown in Figure 5.3-19. The operation is similar to that of a magnetic amplifier[1].

First consider control current I_C of Figure 5.3-18 set at position "a" in Figure 5.3-19. When transistor Q_1 is turned off, the flux in the core of ST_1 drops from positive saturation to position "a" of the B-H curve. This drop in flux is called flux reset (Reference 1). When Q_1 is turned on by a trigger pulse, the flux of ST_1 is driven from position "a" to positive saturation by current flowing in the primary winding (PRI Figure 5.3-18). Q_1 is held "full on" (collector-emitter voltage $\leq$ 0.5 volts) while the flux of ST_1 rises from "a" to saturation. Once ST_1 saturates, Q_1 is turned off and ST_1 resets to position "a".

When I_C is raised to position "b", the flux of ST_1 resets to position "b" on the B-H curve. The operation is the same as it was with I_C at "a" except the flux excursion from "b" to saturation is larger than from "a" to saturation. This leaves Q_1 turned on a longer period of time and E_O is greater at position "b" than at position "a". Likewise as I_C increases to position "c", the flux excursion increases and in turn E_O increases.

The circuit of Figure 5.3-18 is designed so that transistor Q_1 would stay turned on for a full cycle or 1.0 milliseconds (assume 1KC operation although the circuit may be designed for any frequency) if the flux of ST_1 was reset to negative saturation. While Q_1 is turned on, the flux of ST_1 rises at almost a constant rate. Voltage e_{be} of Figure 5.3-18 is held almost constant by the base-emitter drop of Q_1. Therefore, the output voltage E_O is proportional to the amplitude of the reset flux $\Delta\phi_R$ and $\Delta\phi_R$ is a function of I_C. Assuming e_{be} constant and neglecting voltage drops of Q_1, D_F and L_F, the output voltage is $(E_O/E_S) = (\Delta\phi_R/\Delta\phi_M)$ where $\Delta\phi_M$ is the max. flux reset. With the idealized B-H curve, the circuit of Figure 5.3-18 would operate satisfactorily from $E_O \cong 0$ to $E_O \cong 0.95\ E_S$.

The output voltage E_O cannot reach $E_O = E_S$ even with the idealized B-H curve (Figure 5.3-19). For $E_O = E_S$, transistor Q_1 must be turned on 100 percent of the time. If Q_1 stays "on", there is no time for the flux of ST_1 to reset and the circuit could not operate. Even if Q_1 was turned on 98 percent of the time in a cycle and turned off 2 percent of the time, the flux would have to reset too rapidly. Then $\Delta\phi_R = 0.98\ \Delta\phi_M$ and for this fast flux resetting, Q_1 base-emitter voltage e_{be} would be excessive and damage Q_1.

The circuit of Figure 5.3-17 operates in the same manner except $E_O > E_S$. With the idealized B-H curve of Figure 5.3-19, the output voltage E_O of Figure 5.3-17 could be controlled between $E_O = E_S$ and $E_O = 20\ E_S$.

Core Materials for ST_1

Ferrite core materials can provide B-H curves similar to the ideal curve of Figure 5.3-19. However, the ferrite core would be much larger than tape wound cores of 50 percent Ni - 50 percent Fe or of 79 percent Ni - 17 percent Fe - 4 percent Mo. The ferrite core material also saturates more remotely than tape core materials. The remote saturating condition causes slower switch of Q_1 than the sharper saturating condition of tape cores.

Tape wound core materials have B-H curves that vary with frequency. In contrast, the ferrite core material has almost the same B-H curve for 100 cps as 100 kc. The variation in the B-H curve with frequency causes the circuit of Figure 5.3-18 to become unstable at $E_O \gtrsim 0.5\ E_S$ and the circuit of Figure 5.3-17 to become unstable at $E_O \gtrsim 2\ E_S$.

Control Circuit Instability (Conditions and Assumptions)

Control circuit no. 1 used in Figures 5.3-17 and 5.3-18 is unstable when a tape wound core is used for ST_1. In Figure 5.3-18 instability results when $E_O \geq 0.5\ E_S$ and in Figure 5.3-17 when $E_O \geq 2\ E_S$. In practice the circuit of Figure 5.3-18 becomes unstable at $E_O \cong 0.45\ E_S$ due to voltage drops in Q_1, D_D, L_F and switching time of Q_1.

When a tape wound core is used for ST_1 the change in flux $\Delta\phi_R$ during reset is a function of the reset time t_R as well as I_C. This action causes the unstable operation at $E_O = 0.5\ E_S$. It is well known that the B-H hysteresis loops of tape wound cores become wider (larger H) as the frequency increases (Reference 3). It is likewise known that the flux in a tape wound core reverses faster when a large current is applied to a winding than it does when a small current is applied to the winding (assume other windings are open circuit). This technique is used by many General Electric Departments and has previously been described (Reference 2).

In the circuit of Figure 5.3-18 the time to reset the flux in the core of ST_1 varies inversely with output voltage E_O. As control current I_C increases, the reset time t_R decreases. Time t_R is the time for the flux of ST_1 to fall from positive saturation to a flux level set by I_C. Time t_R decreases as output voltage E_O increases.

A complete explanation of the instability is complex and includes many non-linear factors. For this reason, simplifying assumptions are made. These assumptions change the results only slightly and their effects are evaluated later.

The assumptions are:

1. During the reset time, the flux change $\Delta\phi_R = I_C\ t_R$ where I_C is in milliseconds.

2. Saturable transformer ST_1 is so designed that $\Delta\phi_R = \Delta\phi_M$ when $I_C = 1.0$ amperes and $t_R = 1.0$ milliseconds, where $\Delta\phi_M$ is the change of flux in ST_1 that occurs when the flux is driven from positive to negative saturation.

3. The d-c hysteresis B-H loop of ST_1 is neglected.

4. The voltage drop of Q_1, D_F and L_F are neglected when they are conducting current.

5. The switching time of Q_1 is neglected.

6. Operating frequency is 1 kc. That is the trigger pulse (Figure 5.3-18) provides a pulse every 1.0 milliseconds.

7. After ST_1 is reset to negative saturation, Q_1 stays turned on for exactly 1.0 milliseconds while ST_1 is returning to positive saturation.

8. While Q_1 is turned on, the flux of ST_1 rises at a constant rate and the flux excursion in ST_1 is directly proportional to the length of time Q_1 is turned on.

In practice assumption (1) is accurate to about 20 percent between $E_O = 0.3\ E_S$ and $E_O = 0.7\ E_S$ as experienced in a circuit of Reference 2. The absence of the d-c loop assumption (3) results in I_C being much smaller than assumption (1) indicates when $E_O < 0.2\ E_S$. Neglecting voltage drops (assumption 4) and neglecting switching times of Q_1 make E_O about 10 percent higher than E_O in practice. The choice of 1 kc frequency and choice for I_C saves bulky constants in the equations. The tested circuit operated at 1.5 kc but the difference between 1.5 kc and 1 kc does not disturb the following results. The choice of I_C may be adjusted to fit any condition by choice of turns of the control winding.

Control Circuit Instability (Operation)

As discussed above, output voltage E_O is directly proportional to the flux change $\Delta\phi_R$ during the resetting interval of ST_1. Using these assumptions $(E_O/E_S) = (\Delta\phi_R/\Delta\phi_M)$ where $\Delta\phi_M$ is the maximum possible change in flux during the resetting time t_R. As assumed above $(\Delta\phi_R/\Delta\phi_M) = I_C t_R$ when I_C is in amperes and t_R in milliseconds. This relation is illustrated graphically in Figures 5.3-20 through 5.3-24.

The intervals of reset time t_R are shown in B-H loops of Figure 5.3-20 where $\Delta\phi_R = \Delta\phi_M$ for all conditions. The item $K_R H$ is used to relate H to I_C during the reset intervals. This is possible because Q_1 (Figure 5.3-18) is turned off during the reset intervals leaving the primary and secondary of ST_1 open. The control winding is the only winding carrying current during the reset time allowing the control current I_C to be directly related to H of the B-H loops of Figure 5.3-20. The left sides of the B-H loops are vertical because I_C is constant and $I_C = K_R H$.

The operation of varying the reset flux amplitude $\Delta\phi_R$ by reset time t_R, with I_C constant, is illustrated in Figure 5.3-21 with $I_C = 1.0$ ampere.

Minor B-H loops of Figure 5.3-22 illustrate actual circuit operation for various output voltages (E_O) as they would occur if stable operation could be obtained. The flux change as reset time t_R varies for $I_C = 1.0$ ampere is illustrated in Figure 5.3-23 and 5.3-24. Here the theoretical condition for the assumptions are compared to the actual characteristic of a core of 79 percent Ni - 17 percent Fe - 4 percent Mo.

Consider $E_O = 0.5\ E_S$ and assume the condition is established and never disturbed. Let $I_C = 1.0$ ampere, $t_R = 0.5$ milliseconds, and $\Delta\phi_R = 0.5\ \Delta\phi_M$ which in turn provides $E_O = 0.5\ E_S$ and Q_1 is turned on for 0.5 milliseconds. Each cycle provides $t_R = 0.5$ ms and the operation is stable. Once the operation is disturbed, however, the circuit becomes unstable.

Assume the supply voltage E_S dropped for one cycle enough to let Q_1 stay on for 0.6 ms and t_R was reduced 0.4 ms for this one cycle. With $t_R = 0.4$ ms, $\Delta\phi_R = 0.4\ \Delta\phi_M$ (Figure 5.3-21, Q_1 remains turned on for only 0.4 ms instead of 0.6 ms which leaves $t_R = 0.6$ ms for the following cycle. On the next cycle, Q_1 is on for 0.6 ms and $t_R = 0.4$ ms. This in essence is the bi-stable operation observed and it continues until another disturbance occurs.

A tabulation is shown in Figure 5.3-25 for five values of I_C. In Figure 5.3-25 the reset time t_R is disturbed by 10 percent and the recovery or instability is shown cycle by cycle for 10 cycles. Any setting of $I_C < 1.0$ amperes which calls for $E_O < 0.5\ E_S$ forces the circuit to return to a stable operation. As E_O approaches $E_O = 0.5\ E_S$, the recovery time becomes longer.

At $I_C = 1.0$ amperes and $E_O = 0.5\ E_S$, any disturbance results in a bi-stable operation. The circuit can remain at any magnitude of a bi-stable operation if it is set up and no further disturbances occur. It is impossible to hold I_C, E_S and the circuit parameters constant enough to maintain a bi-stable operation at any position desired.

A slight increase of I_C to $I_C > 1.0$ amps (calling for $E_O > 0.5\ E_S$) results in a bi-stable operation of $E_O = 0$ to $E_O = E_S$ as shown in the tabulation of Figure 5.3-25. Similar results to those of Figure 5.3-25 are shown in Figures 5.3-26 and 5.3-27 to illustrate the waveforms of the flux of ST_1 and the instantaneous output voltage e_O (before filter L_F and D_F).

In practice, the bi-stable limits are $E_O = 0.3\ E_S$ and $E_O = 0.7\ E_S$ when $I_C > 1.0$ amperes instead of $E_O = 0$ to $E_O = E_S$ as shown in Figures 5.3-24 to 5.3-27. The reduction in the magnitude of the bi-stable operation is caused by the d-c hysteresis B-H loop.

Reaction of the D-C Loop

The action of the d-c hysteresis B-H loop of ST_1 is to reduce the magnitude of the bi-stable operation. The d-c loop does not change the dividing point between stable and unstable operation away from $E_O = 0.5\ E_S$.

Consider the d-c loop shown dotted in Figure 5.3-21. The d-c loop prevents the flux from falling at a constant rate from positive saturation as shown by the dotted curve of Figure 5.3-23. In Figure 5.3-21 the reset flux change $\Delta \phi_R = 0.9 \Delta \phi_M$, for $I_C = 1.0$ amp. and t_R infinite, due to the effect of the d-c loop.

The proximity of the d-c loop limits $\Delta\phi_R$ to $0.8\,\Delta\phi_M$ at $t_T = 0.8$ ms and $I_C = 1.0$ amp. In general, $\Delta\phi_R \cong t_R$, only, when the d-c loop width is small compared to the dynamic B-H loop width. As the d-c loop gets wider, as it approaches negative saturation, the proximity of the d-c loop to the dynamic B-H loop makes $\Delta\phi_R < t_R$ as illustrated in Figure 5.3-23. As a result bi-stable operation is kept between the limits of $E_O = 0.3\,E_S$ and $E_O = 0.7\,E_S$.

The d-c loop is narrow compared to the dynamic loop at B = 0 of the B-H curves of Figure 5.3-21. Also, at B = 0 the d-c loop is very steep (almost vertical). The constants for the equations and experimental data were taken at the point where the resulting flux was crossing B = 0. This reduced the error caused by the B-H loop at the point of transition from stable to unstable operation. In practice the transition point is at $E_O = 0.45\,E_S$ instead of $E_O = 0.5\,E_S$. This discrepancy results from other components.

The reactions of the dynamic and d-c loops are complete. The above factors provide a simplified explanation of the B-H loops as they relate to circuit operation.

Effect of Other Assumptions

Voltage losses in components result in a slight difference between the theoretical transition from stable to unstable operation and the tested transition point. Voltage drop in D_F and L_F causes $(E_O/E_S) \cong 0.95\,(\Delta\phi_R/\Delta\phi_M)$. Voltage drop in the collector-emitter of Q_1 provides an additional decrease in E_O. The switching time of Q_1 takes away about 5 percent of t_R at $E_O = 0.5\,E_S$. These combined losses leave $(E_O/E_S) \cong 0.9\,(\Delta\phi_R/\Delta\phi_M)$.

Proposed Solutions

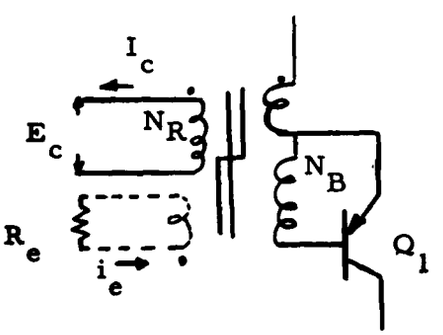
This control circuit can be modified to become stable. As illustrated in Figure 5.3-19 a core material such as ferrite would make this control circuit stable. The use of a ferrite core would increase weight and power loss by increasing switching losses of Q_1. A ferrite core is affected by temperature more than a tape wound core.

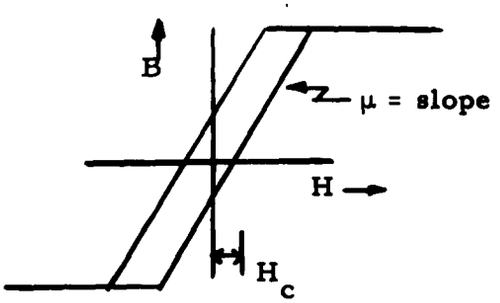
A more promising technique is provided by restricting the maximum time for reset t_R. This technique is described in section 5.3.6 of this report and is called Control Circuit No. 2.

Approximate Analytical Stability Analysis

The previous paragraphs contain a combined quantitative and qualitative explanation of the instability noted in control circuit no. 1. It is also possible to apply control circuit stability criteria to simplified versions of this control circuit and show that instability will occur when $t_{on}/t_{off} > 1.0$. The following paragraphs present this analysis.

The circuit of Figure 5.3-17 will be used for reference. In this case power transistor Q_1 is turned on by a pulse applied to base. Transistor Q_1 turns off when saturable transformer ST_1 saturates. Flux reset is accomplished by a reset current, I_c, during the time transistor Q_1 is off. The flux reset as a function of reset current (I_c) and time (t) will first be determined. It will be assumed that the saturable reactor can be represented as having a core material with B-H characteristic as shown below and a shorted turn to simulate the eddy current and other dynamic losses. The equations describing the operation of this reactor during reset may now be written.





B-H Curve

The only active windings during this time are the reset winding (N_R) and single shorted turn (dotted). It will be assumed that no leakage flux exists so that all flux links both the shorted turn and the reset winding. Thus, the current (I_c) is:

$$I_c = + \frac{H_c \ell}{N_R} - \frac{B \ell}{\mu N_R} \quad i_e$$

where: ℓ = length of magnetic path

Also let:

$$\phi_R = \phi_m - B A_c$$

where: A_c = core area

ϕ_m = total flux at saturation

ϕ_R = total amount of flux reset from saturation

Eliminating B from the previous two equations yields:

$$I_c = + \frac{H_c \ell}{N_R} - \frac{(\phi_m - \phi_R)\ell}{\mu A_c N_R} + i_e$$

The current in the shorted turn is:

$$i_e = \frac{1}{R_e} \frac{d\phi_R}{dt}$$

Eliminating current i_e from the previous two equations gives:

$$I_c = -\left[\frac{\phi_m \ell}{\mu A_c N_R} - \frac{H_c \ell}{N_R}\right] + \frac{\ell \phi_R}{\mu A_c N_R} + \frac{1}{R_e} \frac{d\phi_R}{dt}$$

Solving this differential equation yields:

$$\phi_R = K_1 \left[1 - e^{-t/\tau}\right]$$

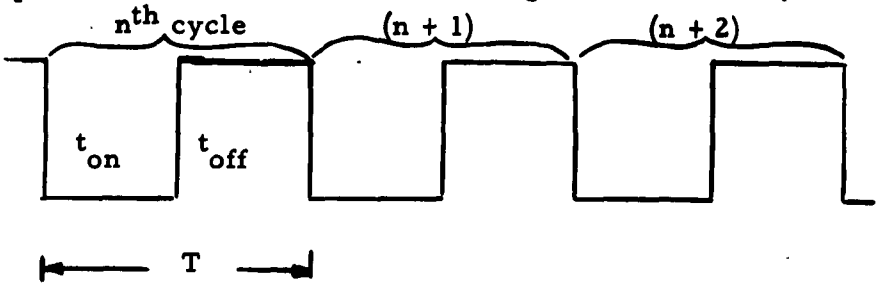
where: $K_1 = \frac{\mu A_c N_R}{\ell} I_c + \phi_m - \mu H_c A_c$

$$\tau = \frac{\mu A_c N_R}{\ell R_e}$$

Reset stops at the end of the reset part of the cycle when $t = t_{off}$; thus at this point:

$$\phi_R = K_1 \left[1 - e^{-\frac{t_{off}}{\tau}} \right]$$

Let it be assumed that the wave form of emitter-collector voltage of power transistor is of the following form. Three cycles are



shown beginning with the n^{th} cycle. It is evident that the amount of flux reset occurring during the n^{th} cycle is:

(a) $$\phi_{R(n)} = K_1 \left[1 - e^{-\frac{t_{off(n)}}{\tau}} \right]$$

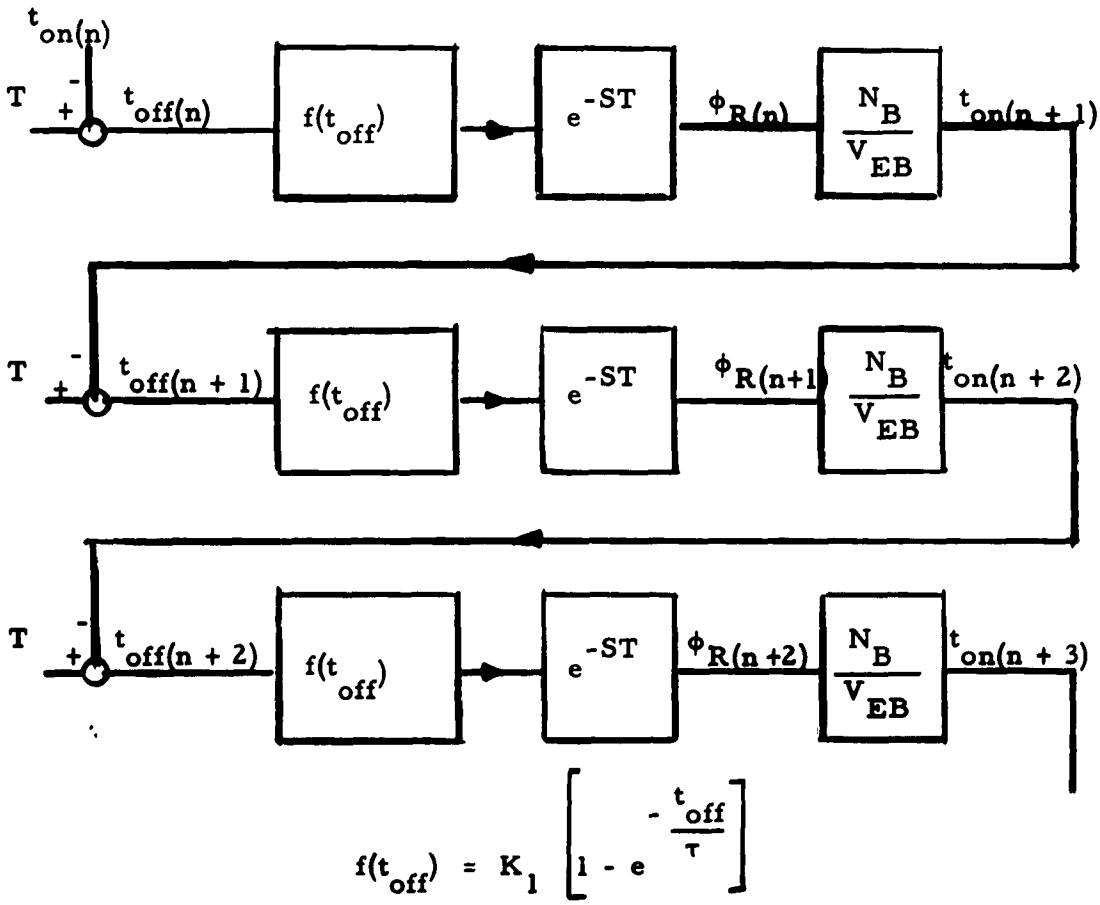
It will be assumed that during the on portion of the cycle the emitter-base voltage is constant at a value of V_{EB}. The on time for the (n + 1) cycle is proportional to the flux reset occurring during the n^{th} cycle. Thus:

(b) $$t_{on(n+1)} = \frac{N_B \phi_{R(n)}}{V_{EB}}$$

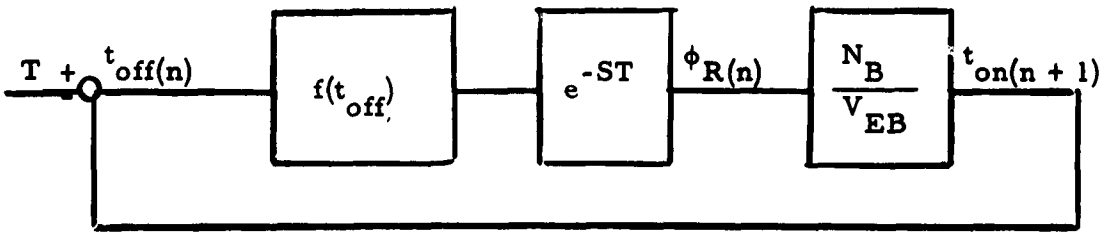
Of course the time off for the n^{th} cycle is:

(c) $$t_{off(n)} = T - t_{on(n)}$$

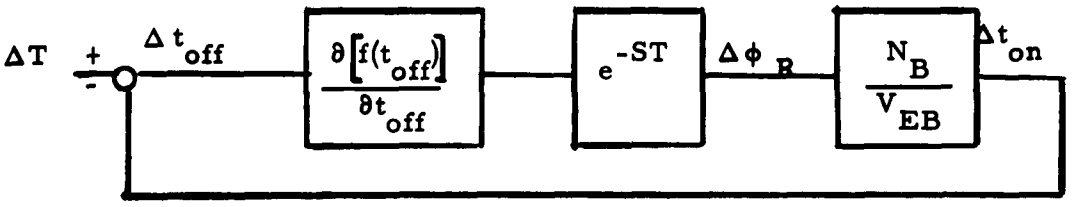
Time-wise, the flux reset $\phi_{R(n+1)}$ at the end of (n + 1) cycle is determined a time, T, after the flux $\phi_{R(n)}$ for the n^{th} cycle is known. This delay can be represented as a transportation lag of T seconds given by e^{-ST} where S is the LaPlacian operator. This time delay plus the relations of a, b, c can be represented in a block diagram such as follows. This defines the control circuit behavior beginning at the start of n^{th} cycle and going through the (n + 3) cycle. This block diagram could be continued to represent as many cycles as desired. However, the same result can be achieved with a single block diagram in which the output is fed back to the input as shown in the next figure. This representation would simulate operation by computing various cycle quantities consecutively for each cycle with a time delay of T seconds between computation.



$$f(t_{off}) = K_1 \left[1 - e^{-\frac{t_{off}}{\tau}}\right]$$



The stability of the preceding loop will now be examined. In order to do so small variations about a given operating point will be considered. For this condition, the above block diagram becomes:



where: $$\frac{\partial [f(t_{off})]}{\partial t_{off}} = \frac{K_1}{\tau} \quad e^{-\frac{t_{off}}{\tau}}$$

A loop such as this will be stable only if:

$$\frac{N_B K_1}{V_{EB} \tau} \quad e^{-\frac{t_{off}}{\tau}} \quad < 1.0$$

However, from relationships a and b:

$$\frac{N_B K_1}{V_{EB}} = \frac{t_{on}}{\left(1 - e^{-\frac{t_{off}}{\tau}}\right)}$$

Thus the criteria for stability becomes:

$$\frac{t_{on}\, e^{-\frac{t_{off}}{\tau}}}{\left[1 - e^{-\frac{t_{off}}{\tau}}\right]\tau} < 1.0$$

or

$$(d) \qquad \frac{t_{on}}{T} < \frac{\left[e^{+\frac{t_{off}}{\tau}} - 1\right]\tau}{T}$$

In the case of laminated iron core material, the value of τ will be large compared to t_{off}. For this case

$$e^{+\frac{t_{off}}{\tau}}$$

is approximately equal to $1 + t_{off}/\tau$; thus from equation (d) the condition for stable operation is:

$$\frac{t_{on}}{T} \leq \frac{t_{off}}{T}$$

This result checks with the result obtained experimentally.

If a ferrite core material could be used, there would be very little eddy current loss; i.e., the value of R_e for the equivalent shorted turn would be large. As a result τ could be small compared to t_{off}. In particular, if τ were zero then relationship (d) states that for stable operation:

$$\frac{t_{on}}{T} \leq \infty$$

This agrees with previous conclusions which stated that the circuit could be stable if the dynamic B-H curve were the same as the DC one.

5.3.6 Control Circuit #2

Control circuit #2 is shown in Figure 5.3-28. This control circuit operates similarly to control circuit 1 described above except for the use of a clock circuit and a unijunction (Reference 4) timing circuit makes it stable from $E_0 = E_S$ to $E_0 > 4E_S$.

The power circuit operation showing the functions of L_F, D_F, C_F and Q_1 was described earlier in this report. The operation of ST_1 and Q_1 to control the power is different in control circuit #2 than in circuit No. 1. This part of this report presents the operation of power transistor (Q_1) the saturable transformer, (ST_1) the clock circuit, and the unijunction timing control.

Power Transistor Operation

The power transistor Q_1 of Figure 5.3-28 is operated as a switch by the saturable transformer ST_1. The operation of Q_1 and ST_1 is illustrated in Figure 5.3-29. ST_1 is reset to negative saturation while Q_1 is turned off, but ST_1 does not saturate while Q_1 is turned on.

Transistor Q_1 is turned on by a pulse of current i_{ON} which is applied for approximately ten microseconds. After i_{ON} is removed, Q_1 is held "on" by base current i_b which is supplied by the secondary (SEC) of ST_1. Q_1 remains "on" until the inhibit transistor Q_{IH} is turned on. With Q_{IH} "on", inhibit current i_{IH} reduces base current i_b to such a low value that Q_1 turns off. (Reference 5). With Q_1 "off," reset current i_R is applied for 100 microseconds and the flux of ST_1 is reset to negative saturation. After ST_1 is reset, i_R is removed, a delay time t_D follows, and then a pulse of current i_{ON} is reapplied for ten microseconds. The operation continues. The phase relations of the currents of Figure 5.3-29 are shown in Figure 5.3-30. ST_1 is reset to negative saturation each cycle. The length of time i_R is applied is constant and the time to reset ST_1 does not influence E_0 as it did in control circuit No. 1. Therefore, this circuit is stable at $E_0 < 2E_S$.

The operation of Q_1 is controlled by the length of time t_D that current i_{ON} is delayed from the time reset current i_R is removed. If $t_D = t_{CM}$ the maximum range of control time, Q_1 remains turned off and $E_0 = E_S$ (neglecting voltage drop of D_F). If $t_D = 0$, the time that Q_1 is turned on is $t_{ON} = t_{CM}$ and E_0 is maximum. By controlling t_D the output voltage E_0 is controlled from $E_0 = E_S$ to the maximum value of E_0.

The output voltage $E_0 = E_S + E_S (t_{ON}/t_{OFF})$ where t_{ON} is the length of time Q_1 is on and t_{OFF} is the length of time Q_1 is off ($t_{OFF} = t_R + t_D$). E_0 is minimum when $t_{ON} = 0$ and E_0 is maximum when $t_{OFF} = t_R$ (the length of time reset current i_R is applied and $t_{ON} = t_{CM}$. Theoretically E_0 could be as large as $E_0 = 5.7E_S$ if power losses in L_F, D_F, Q_1 and ST_1 were neglected for an operating frequency of 1.5 KC and $t_R = 100$ μS. In practice E_0 is maximum at $E = 4E_S$ allowing for losses and that t_R cannot be reduced to zero.

The operating frequency (1.5 KC) and reset time t_R is determined by the clock circuit (Figure 5.3-31). The delay time is determined by the unijunction timing control (UTC) shown in Figure 5.3-32). By the UTC controlling t_D from $t_D \cong 0$ to $t_D = t_{CM}$, the UTC controls t_{ON} and in turn controls E_0.

Clock Circuit

The clock circuit is shown in Figure 5.3-31. The clock sets the frequency. The clock also turns off the power transistor Q_1 by providing the inhibit function of Q_{IH}, resets ST_1, and initiates the start of the unijunction timing control (UTC) of Figure 5.3-32. The connections of the clock to the power circuit and UTC are shown in Figure 5.3-33.

The clock is a saturable transformer-transistor oscillator similar to a miniature version of the power circuit Figure 5.3-29. The operation of the circuit used for the clock has previously been described[2]. A brief description is presented here for this report.

The clock timing circuit transistor Q_T of Figure 5.3-31 is partially turned on by bias resistor R_T1 and R_T2. As Q_T turns on, saturable transformer ST_T (positive at dots) drives Q_T "full on" similar to the operation of ST_1 and Q_1. Transistor Q_T remains "on" until ST_T reaches positive saturation (different from ST_1). When ST_T saturates, Q_T turns off. After Q_T turns off, current through resistor R_T2 and the reset winding of ST_T forces the voltages of ST_T to reverse (negative at dot). With ST_T negative, Q_T is held "off" while the flux of ST_T core is driven from positive to negative saturation. Once ST_T reaches negative saturation, the negative voltage of ST_T windings drop to zero and Q_T is turned on, again, by R_T1 and R_T2. The oscillation continues.

The length of time Q_T is "on", is determined by the SEC winding of ST_T, the voltage drops of resistor R_{T1} and the base to emitter of Q_T. The time Q_T is turned "on" is approximately 100 microseconds as set mainly by the design of ST_T. This time is the length of time for ST_T to move from negative to positive saturation.

The length of time that Q_T is turned off is the time for ST_T to reset (flux move from positive to negative saturation). The reset time is determined by diode D_T and the design of ST_T. The forward voltage drop of D_T (a silicon diode) limits the voltage across the reset winding during the time of reset. With the reset winding voltage constant, the rate of change of flux is constant ($d\phi/dt$). With the flux change $\Delta\phi$ constant (positive to negative saturation of ST_T), the time for reset is constant ($\pm$ 10%). The reset time is set for 570 microseconds as determined by the design of ST_T which sets the clock frequency at 1.5 KC. The time Q_T is turned on provides t_R of Figure 5.3-30; and the time Q_T is turned off provides the time t_{CM} (the max. range of control time).

Unijunction Timing Control

The unijunction timing control (UTC) determines the repetition rate that power transistor Q_1 is turned on. The UTC is same as a unijunction oscillator circuit except diodes D_{S1} or D_{S2} are used to inhibit the oscillation. The unijunction oscillator has previously been described (Reference 4) and is not repeated here.

If diodes D_{S1} and D_{S2} were removed, the UTC would oscillate at a frequency set by the resistance of the collector-emitter of Q_C and the capacitance of C_C. The frequency could be controlled over a wide range of frequency by varying E_C, the base-emitter voltage of Q_C. When diode D_{S1} is connected across C_C the oscillation of UTC is inhibited. With the cathode of D_{S1} connected to the emitter of Q_T of the clock (Figure 5.3-32), UTC is inhibited when Q_T is turned on during time t_R. While Q_T is "on", capacitor C_C is discharged and the timing function of UTC is reset. This operation synchronizes the UTC with the clock and allows the UTC to provide one timing period for t_D during each cycle as shown in Figure 5.3-30. After each timing period t_D, Q_{UT} "fires" and discharges C_C through the base-emitter of Q_{ON}. This operation turns on Q_{ON} for approximately ten microseconds and turns on Q_1 of the power circuit. After Q_1 is turned on, D_{S2} inhibits the UTC and oscillation is prevented until after Q_1 is turned off. The UTC times for the interval of time t_D and the UTC is inhibited during time intervals t_{ON} and t_R.

The timing interval t_D is controlled by voltage E_C. Time $t_D \cong R_{ce}C_C$ where R_{ce} is the resistance of the collector-emitter of Q_C and C_C is the capacitance of capacitor C_C. The resistance R_{ce} is a function of base-emitter voltage E_C and t_D in turn is controlled by E_C.

The connections of the UTC, the clock, and power circuit are shown in Figure 5.3-33. Controlling transistor Q_C is connected in a zener diode reference bridge. Output voltage E_0 is attenuated by resistors R_1 and R_2 and compared to the voltage of zener diode D_{ZR}. The output voltage E_C of the reference bridge is supplied to Q_C and in turn E_0 is regulated at 28 volts. The voltage across D_{ZR} also supplies the power for the UTC.

Future Work on Control Circuit No. 2

The circuit of Figure 5.3-33 has been built except for the Zener diode reference bridge. A problem of premature turning on of Q_1 occurs when Q_T turns off. This interaction will be corrected by a clipper circuit. This clipper circuit will be built, the Zener bridge added, and the "loop closed."

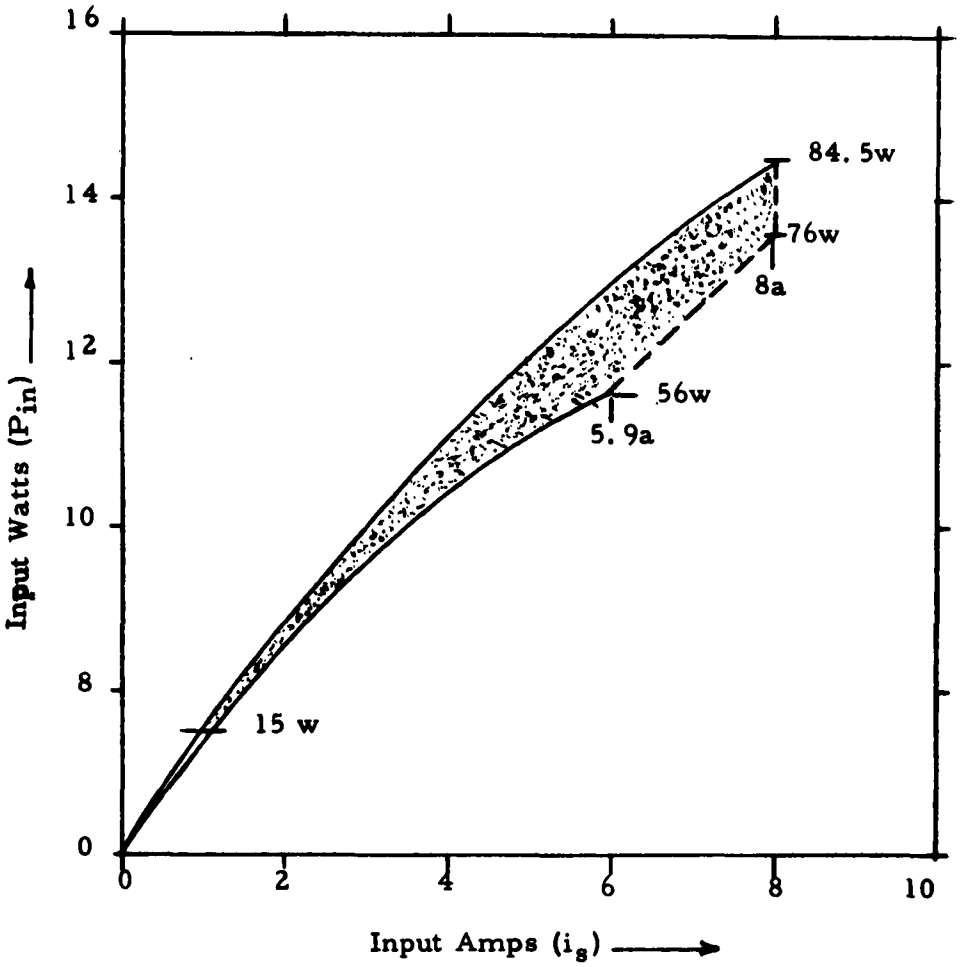


Figure 5.3-1 Converter Input Characteristics

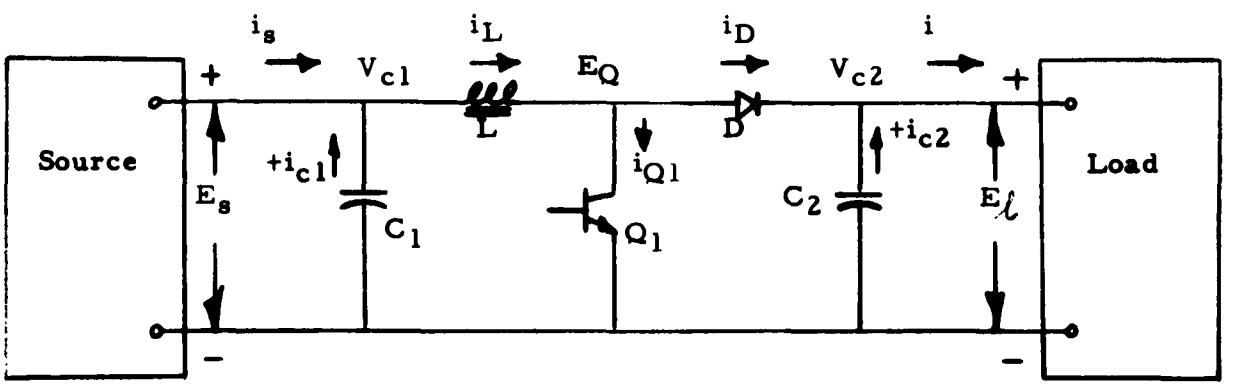


Figure 5.3-2 Basic Fly-Back Circuit

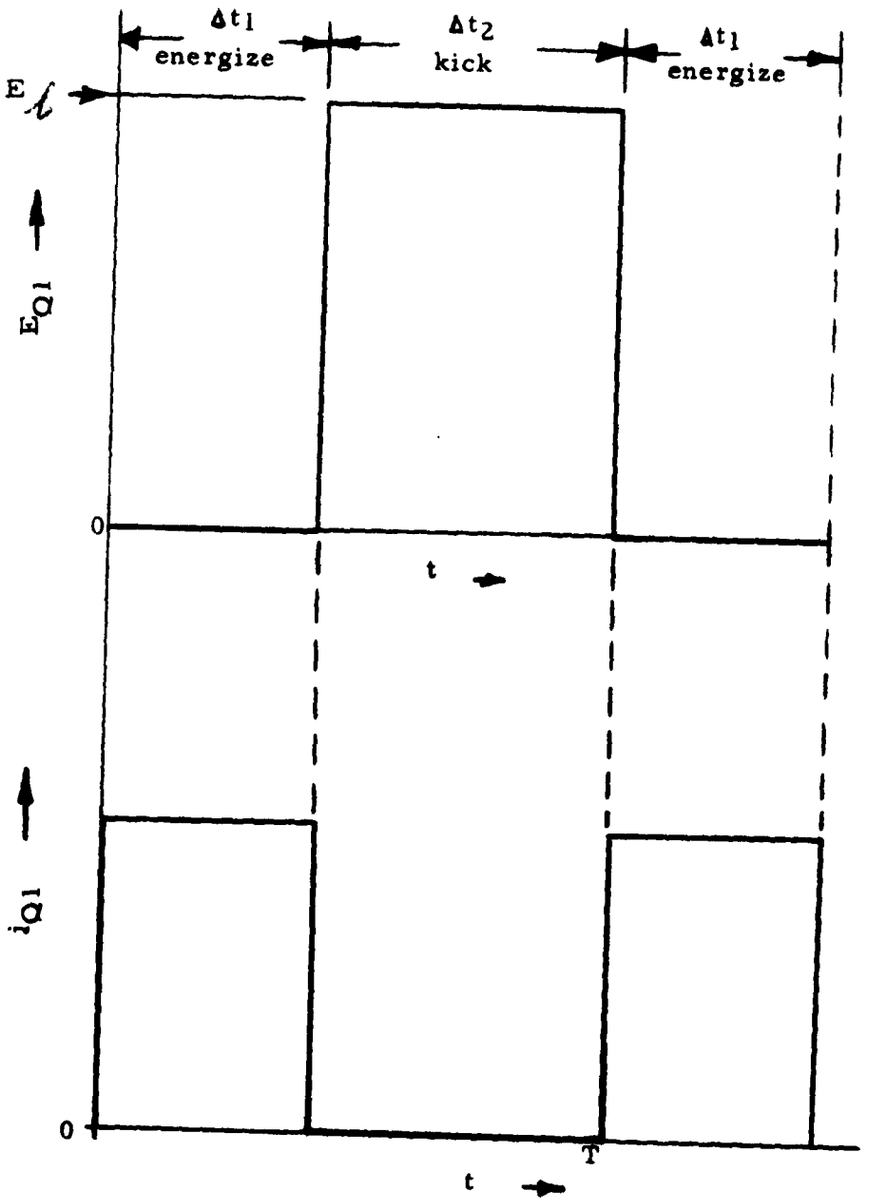


Figure 5.3-3 Full Load Wave Forms

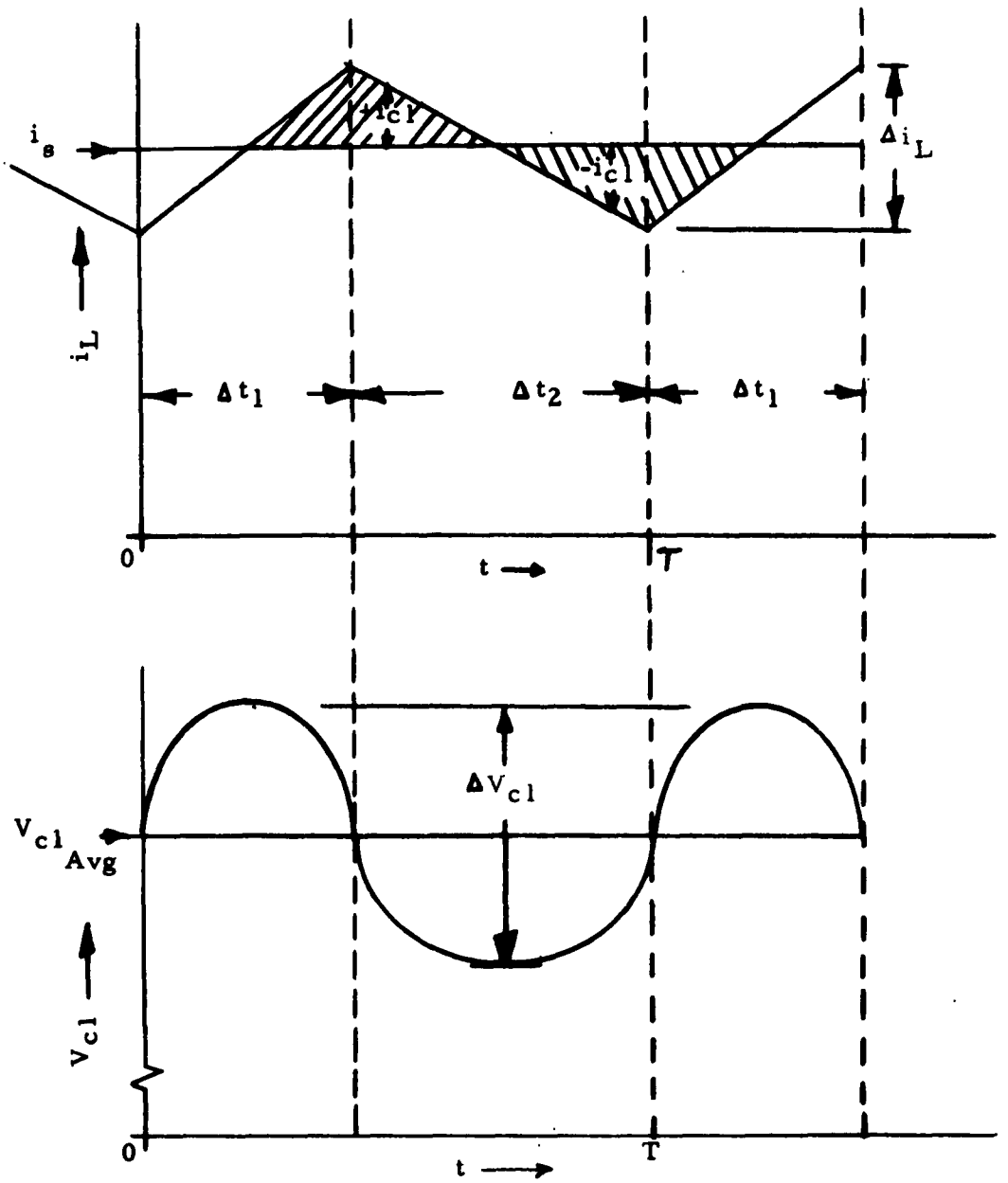


Figure 5.3-4 Full Load Wave Forms

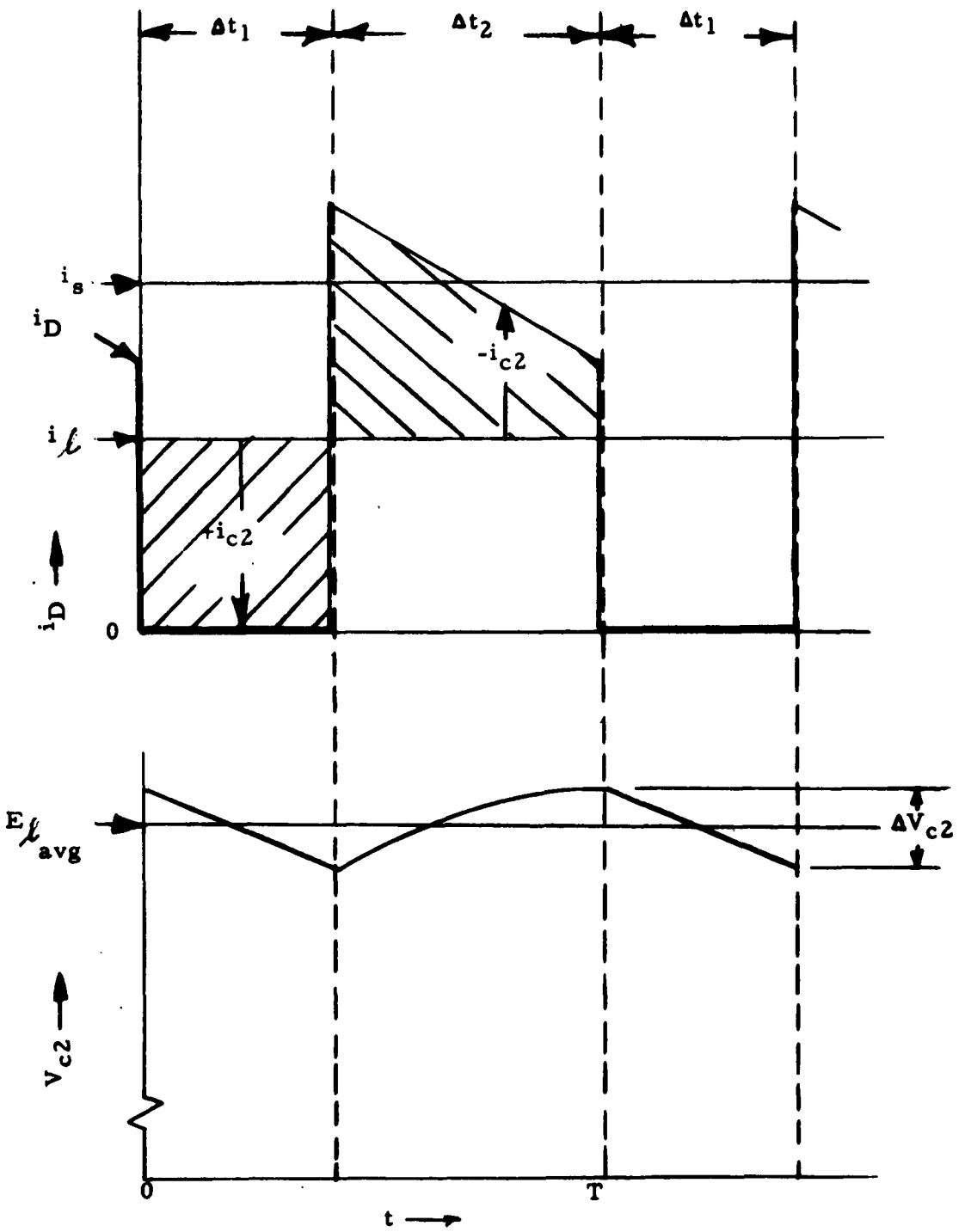


Figure 5.3-5 Full Load Wave Forms

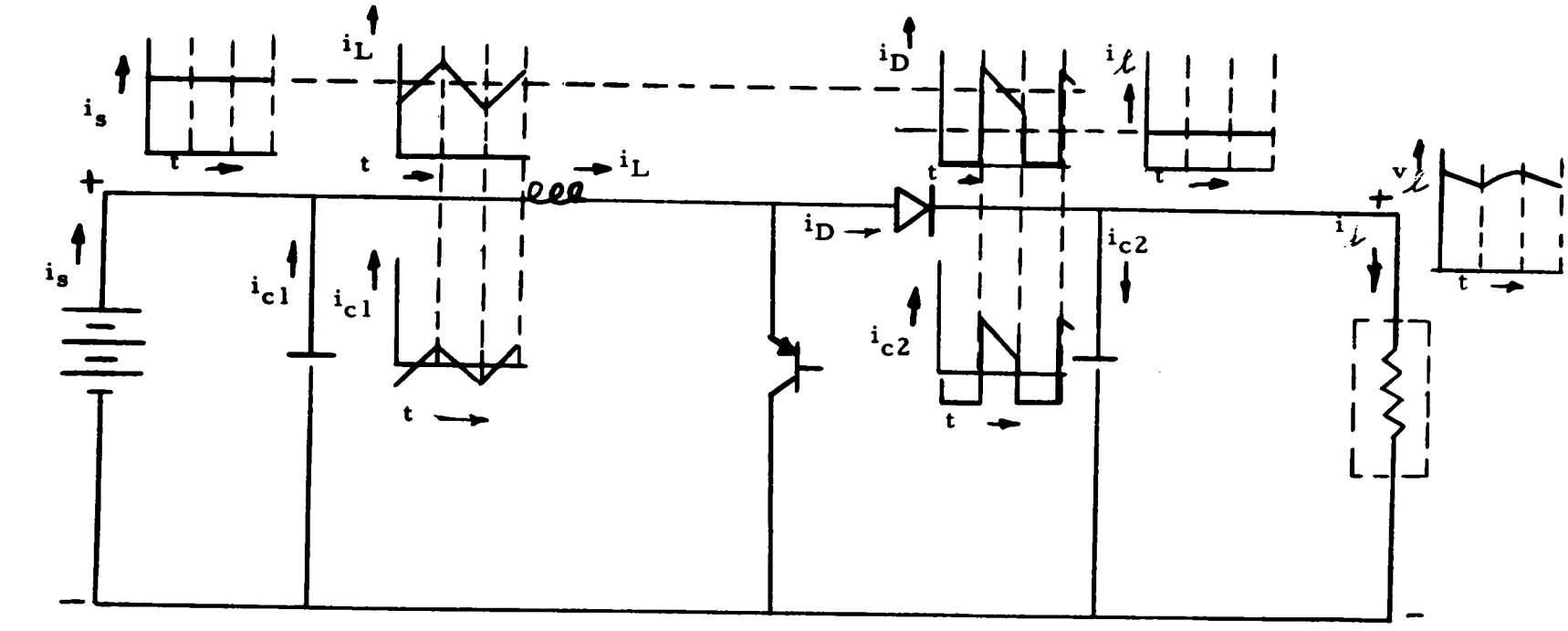


Figure 5. 3-6 Wave Shapes at Full Load

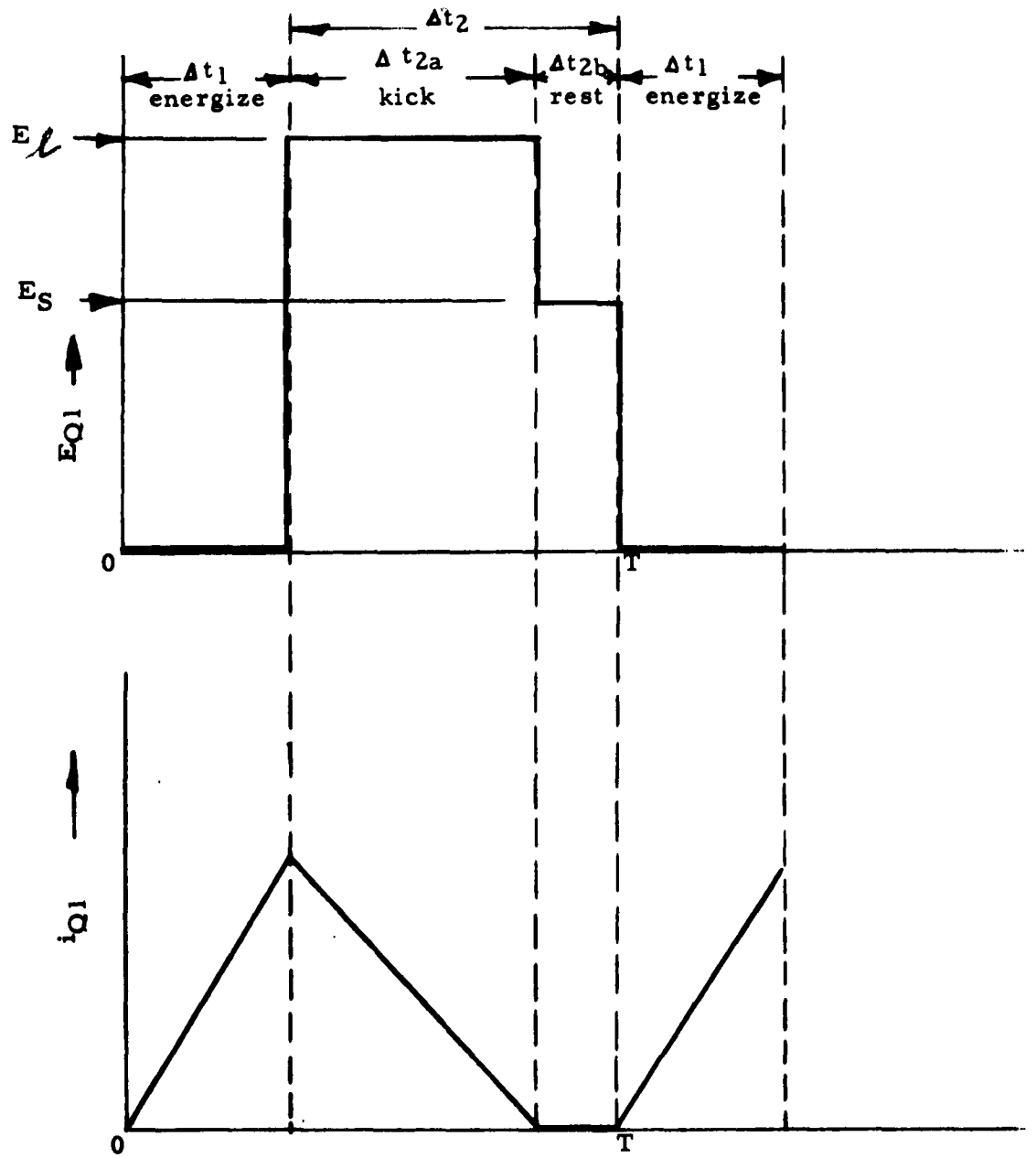


Figure 5.3-7 Light Load Wave Forms

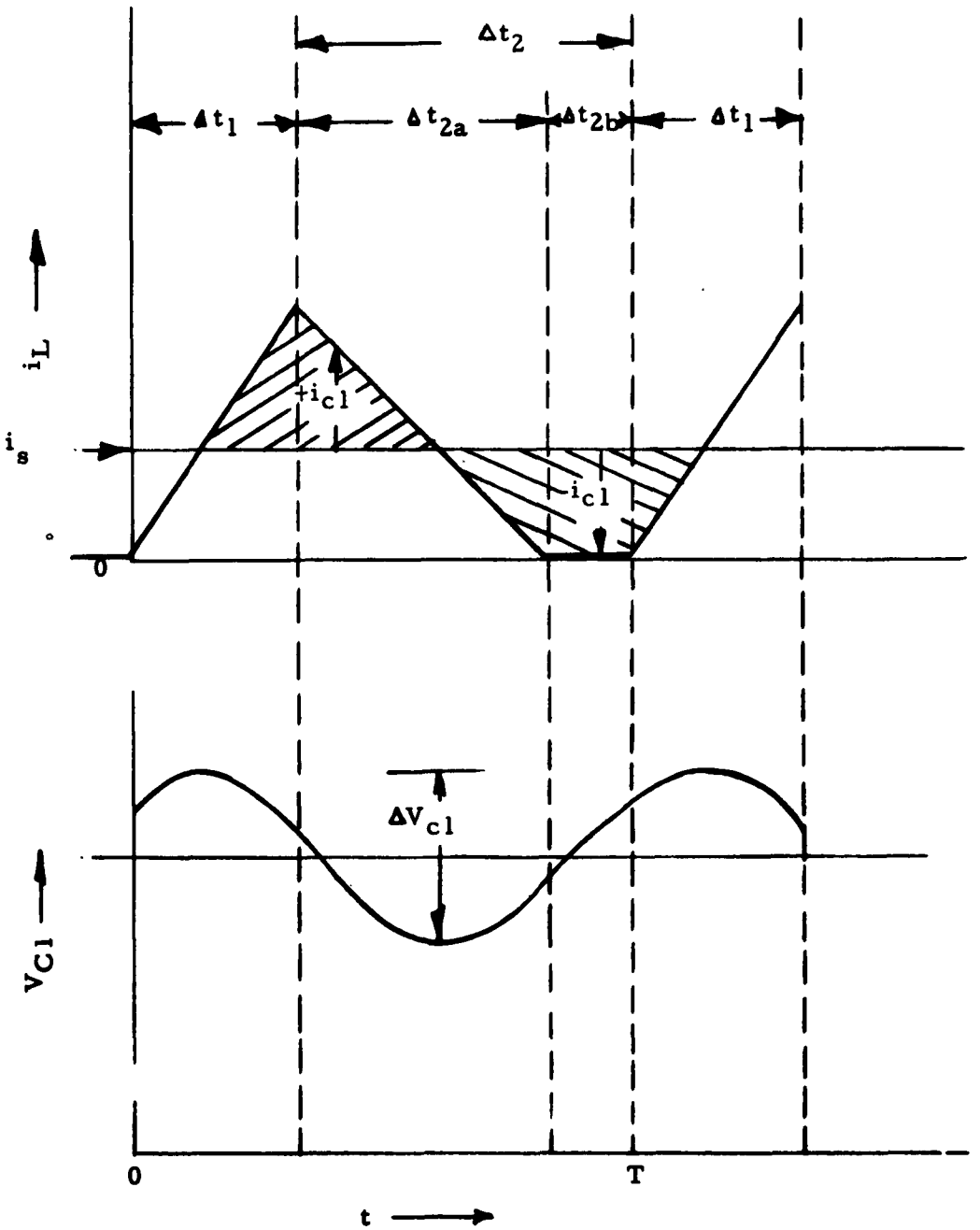


Figure 5.3-8 Light Load Wave Forms

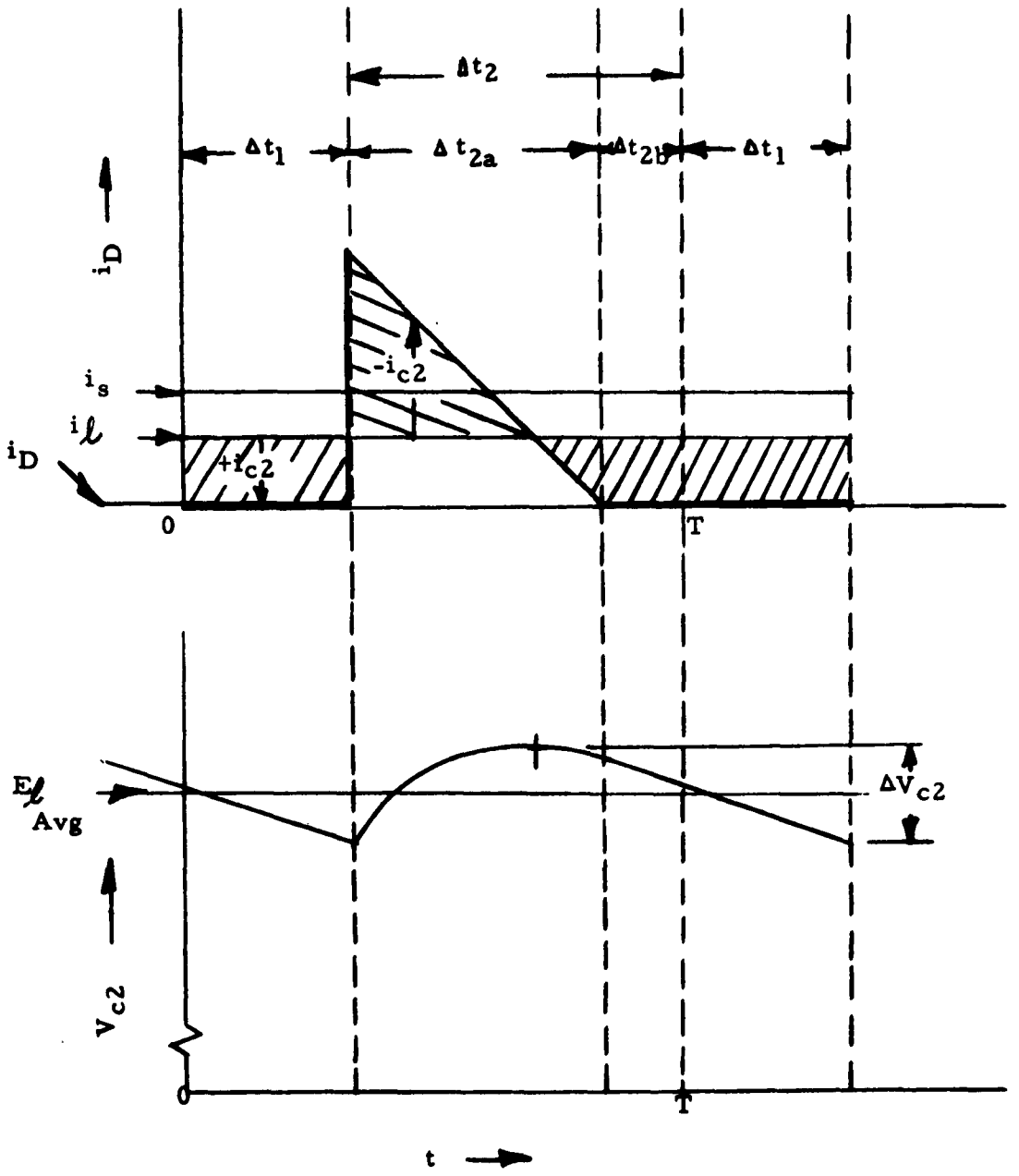


Figure 5.3-9 Light Load Wave Forms

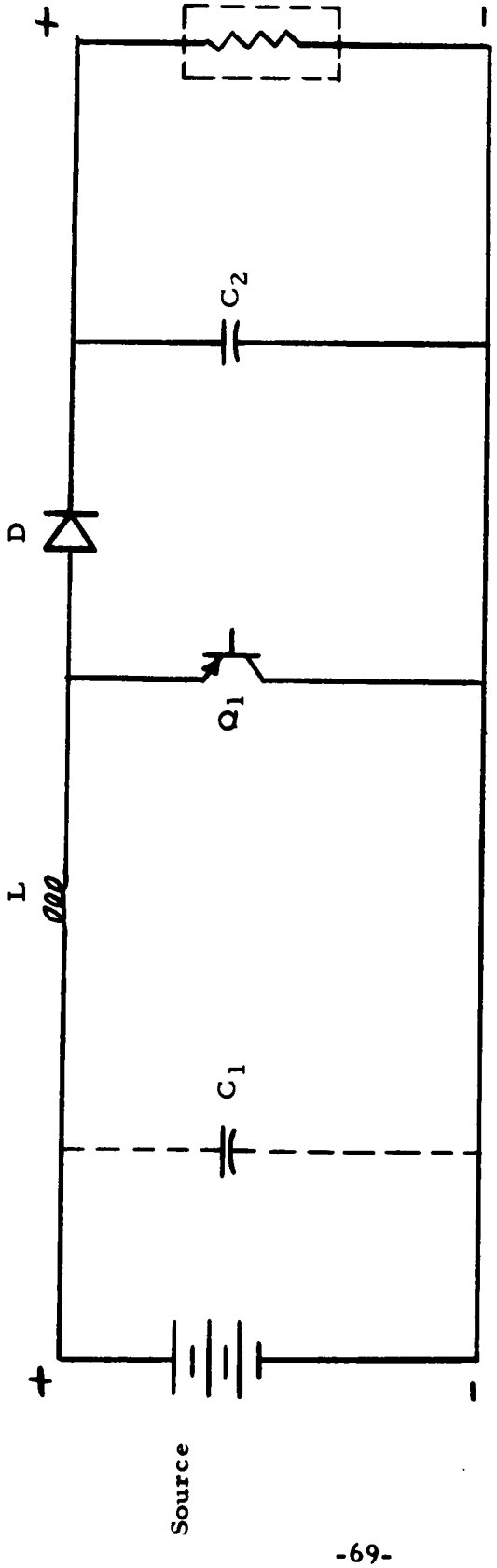


Figure 5.3-10 Basic Flyback Circuit

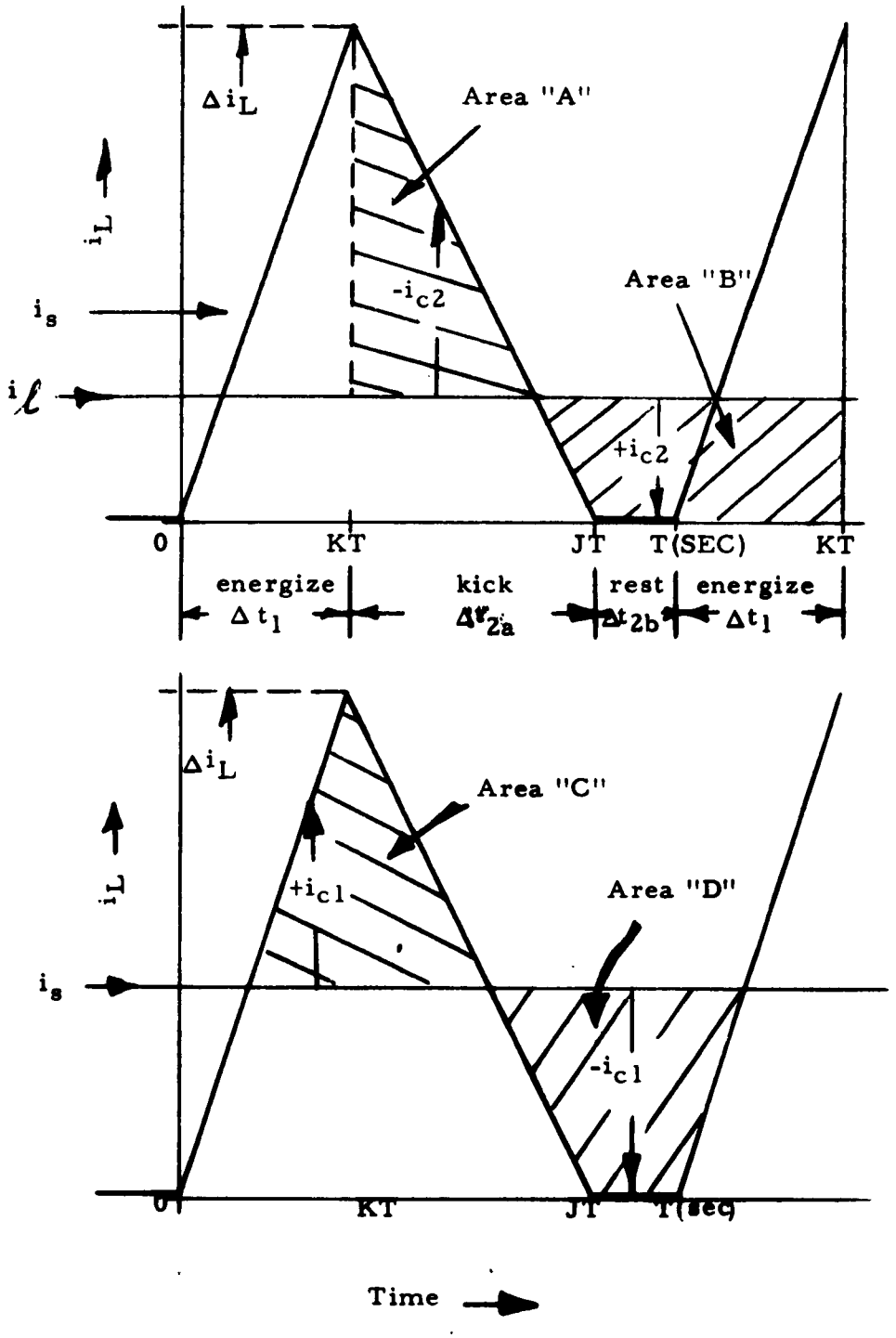
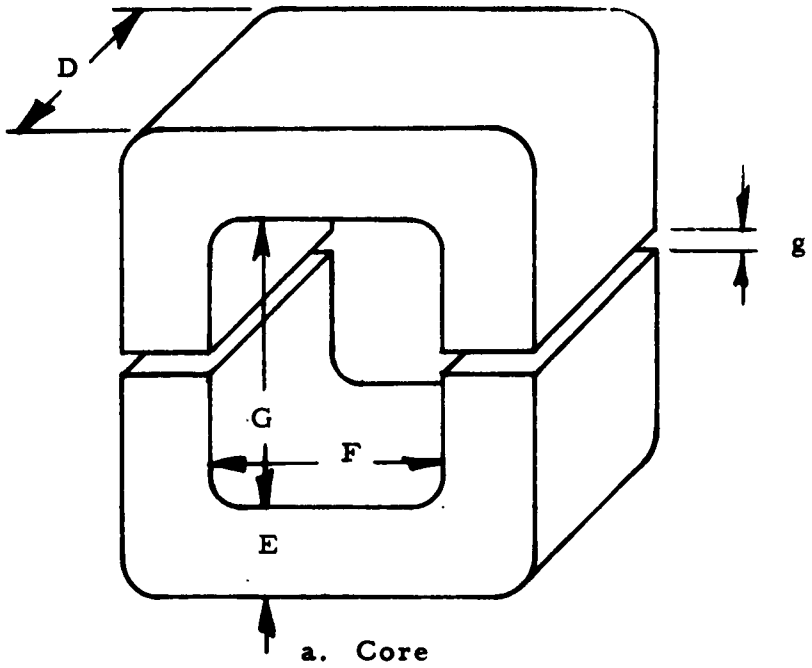
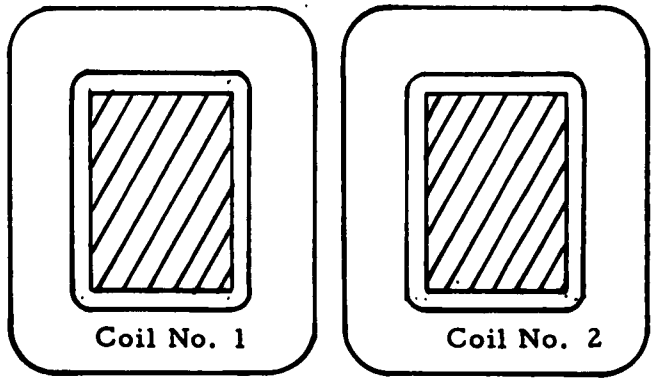


Figure 5.3-11: Light Load Current Wave Forms

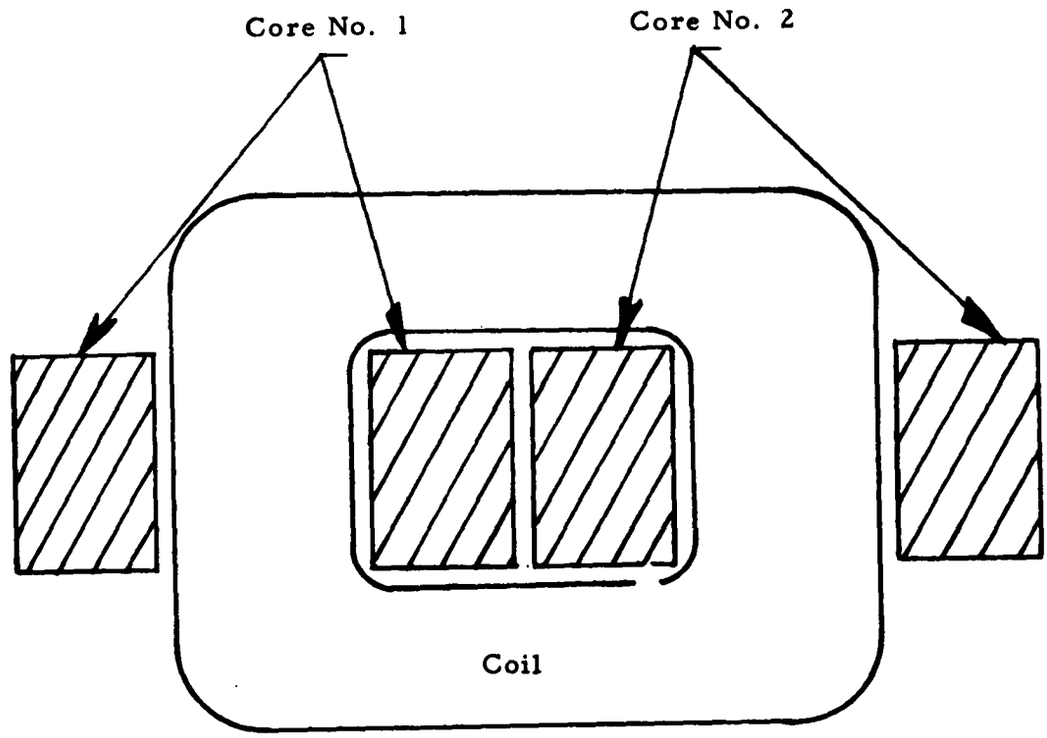


a. Core



b. Cross section at gap - Through Coils

Figure 5.3-12 Single "C" Core - Double Coil



Cross section at gap - Through Coils

Figure 5.3-13 Double "C" Core - Single Coil

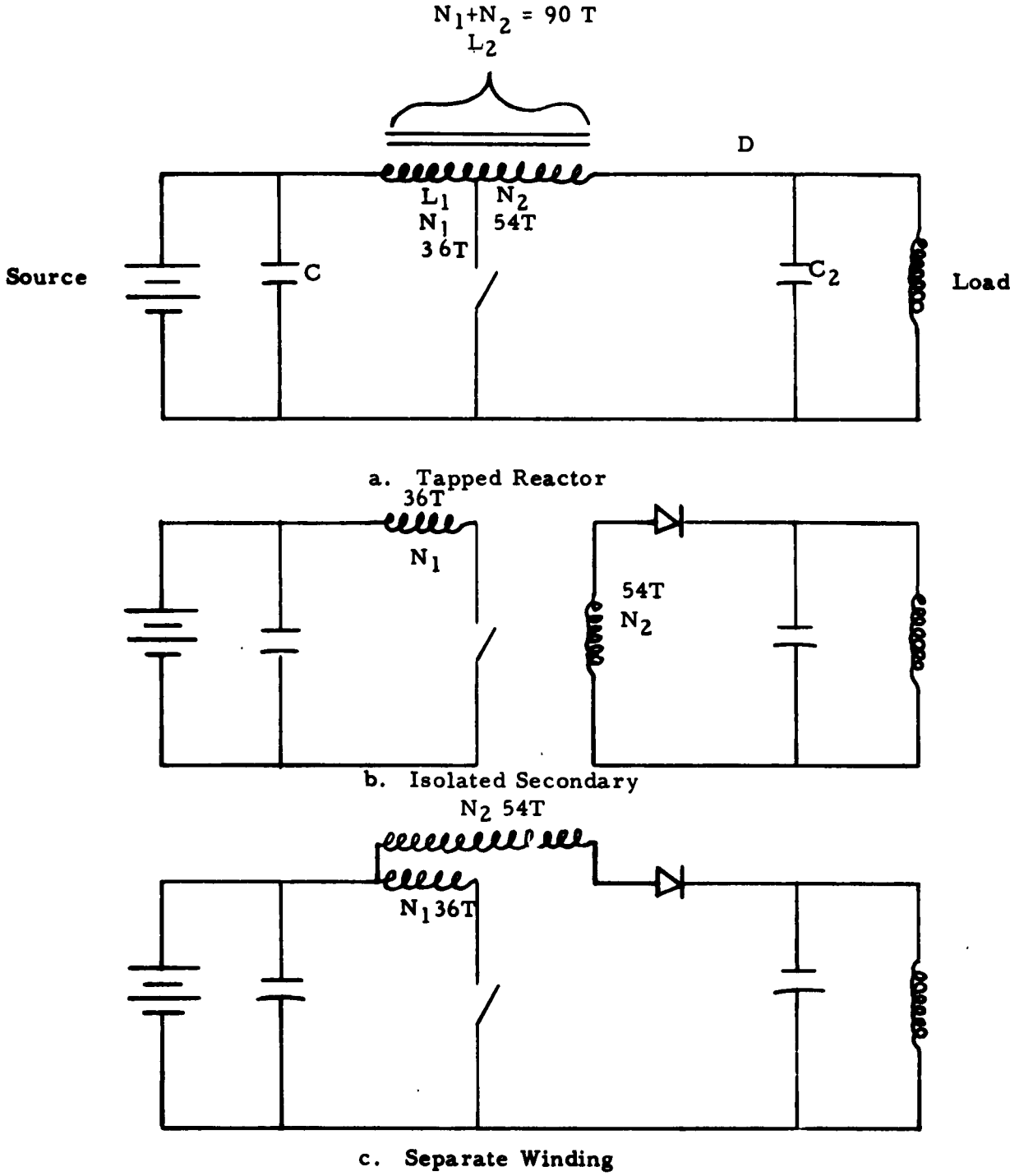
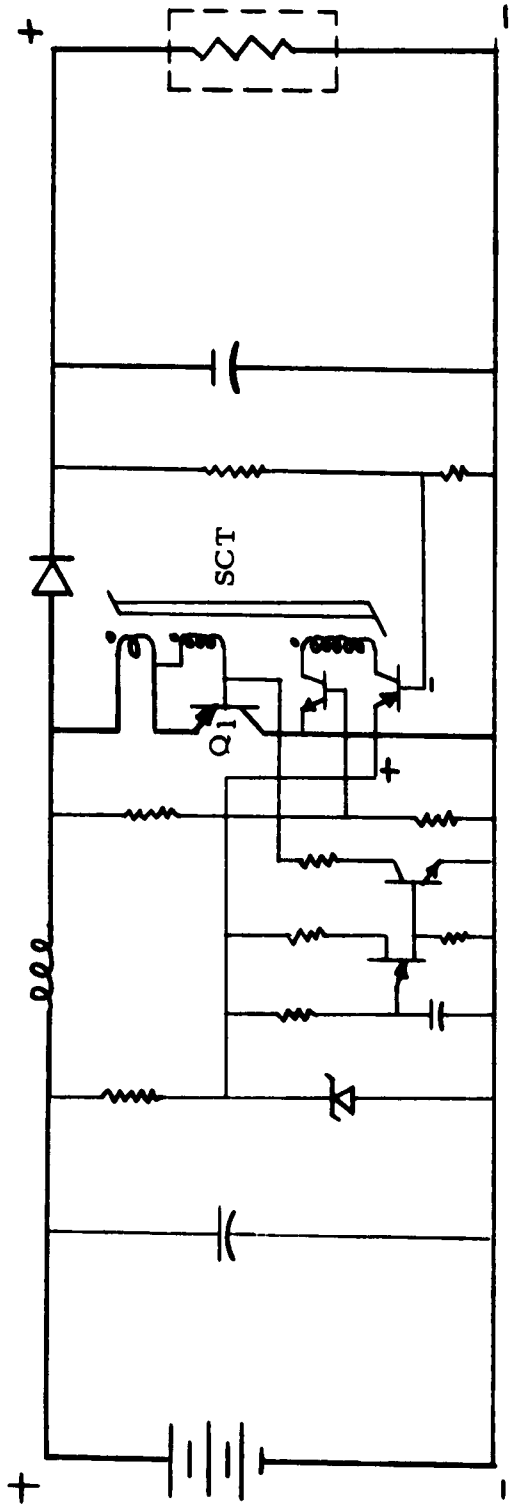


Figure 5. 3-14 Other Power Circuits



Flyback Circuit With Proposed Control No. 1

Figure 5.3-15

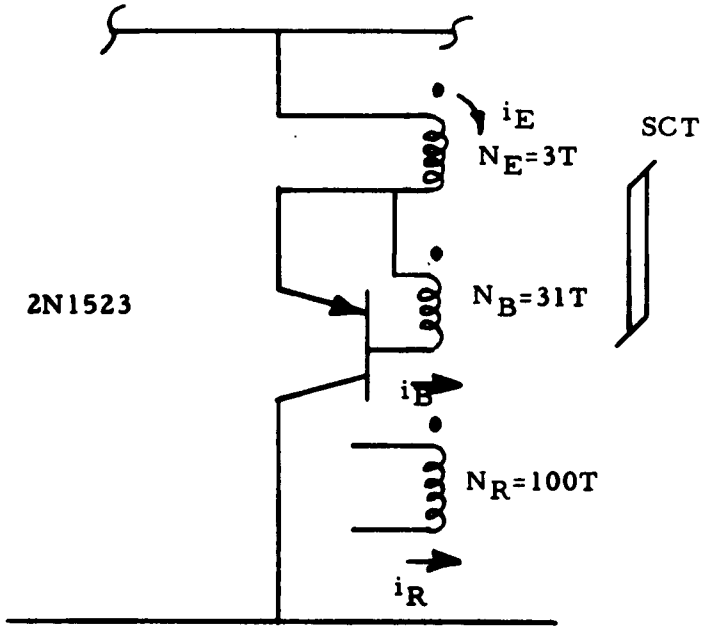


Figure 5.3-16 Simplified Schematic Diagram of Saturable Transformer and Power Transistor

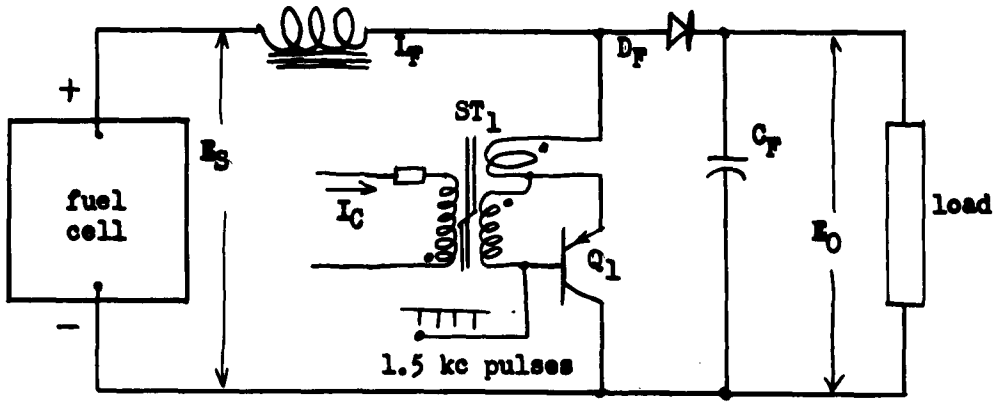


Figure 5.3-17 Basic circuit of control circuit #1 used to step up voltage E_S to provide output voltage $E_0 > E_S$. Control current I_C is supplied by reference and feedback circuit (not shown). This circuit is unstable if $E_L \geq 2E_S$. Bias for Q_1 is not shown.

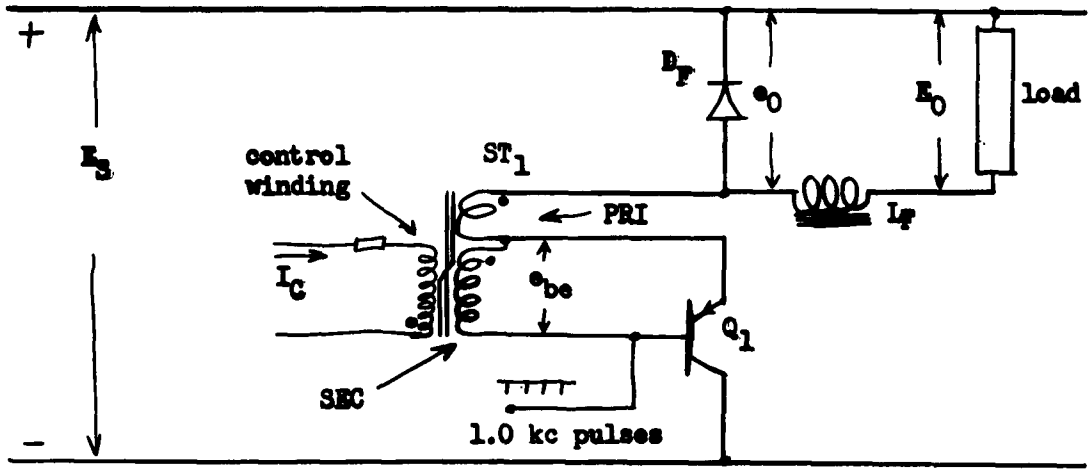


Figure 5.3-18 Control circuit that operates same as Figure 5.3-17 except $E_0 \sim E_S$ in constrast to $E_0 \geq E_S$ of Figure 5.3-17. This circuit is unstable if $E_0 \geq 0.5E_S$. The operation of Q_1 and ST_1 is related to I_C same as in Figure 5.3-17. Here E_0/E_S is a direct function of the ratio of time Q_1 is "on" and independent of load current if the voltage drops of Q_1 and D_F are neglected. It is easier to understand the instability in this circuit but the solution applies equally to Figure 5.3-17.

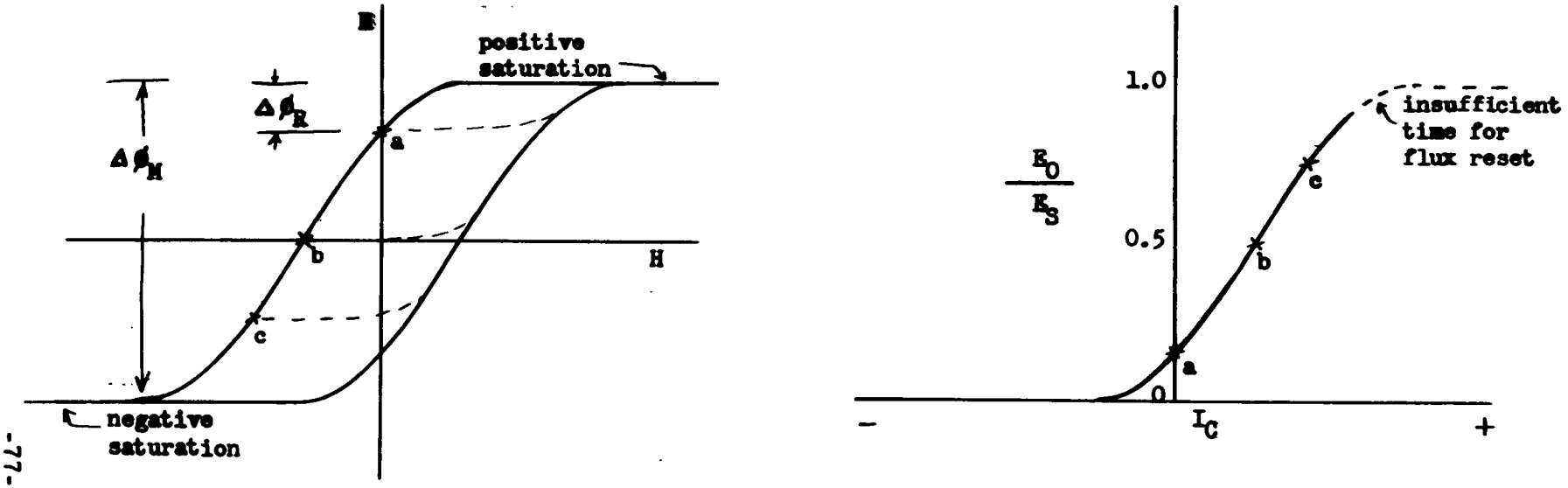


Figure 5.3-19 Idealized major and minor B-H loops of ST_1 and their relation to the transfer characteristic(E_0 vs I_C) of Figure 5.3-18. These B-H loops are similar to those of a ferrite core material but they are not similar to 50% Ni - 50% Fe or 79% Fe - 4% Mo cores. Points a, b, and c relate the flux position at the end of reset to the position of E_0.

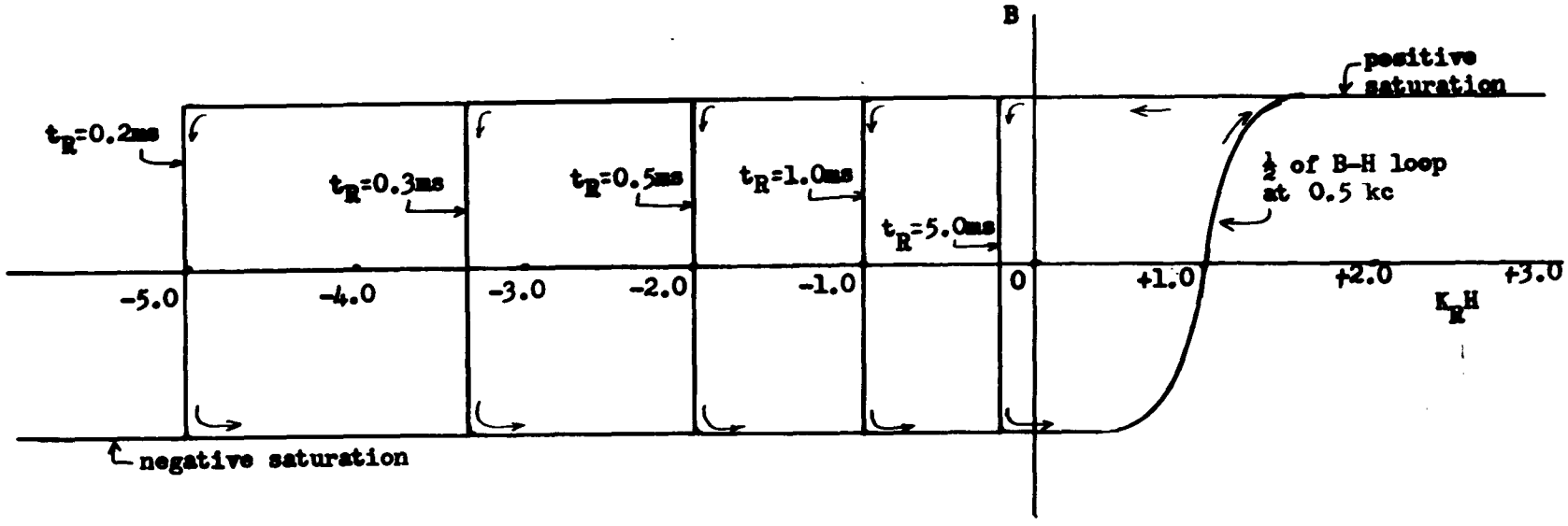


Figure 5.3-20 Theoretical B-H loops for various reset times t_R in milliseconds for ST_1 of Figure to reset the flux of ST_1 to negative saturation for each value of t_R. Term K_R relates H in oersteads to control current I_C during the resetting time of ST_1 where $K_R H = I_C$. The design of ST_1 is assumed to require I_C = 1.0 amps. to reset the core of ST_1 from positive to negative saturation in 1.0 milliseconds. $K_R H$ relates the loops to the equations for explaining the circuit of Figure 5.3-18.

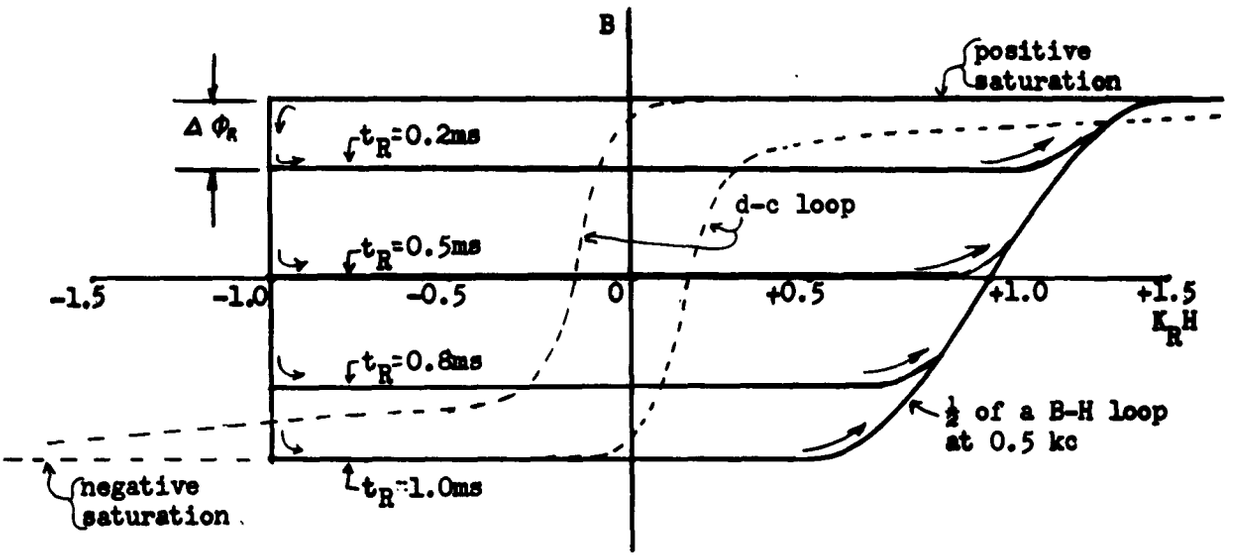


Figure 5.3-21 Theoretical B-H loops for various lengths of reset time t_R with I_C = 1.0 amp., showing the amplitude of flux change $\Delta\phi$ during reset as a function of reset time t_R. D-C loop is shown dotted but the d-c loop is neglected in the operation of the solid line B-H loops.

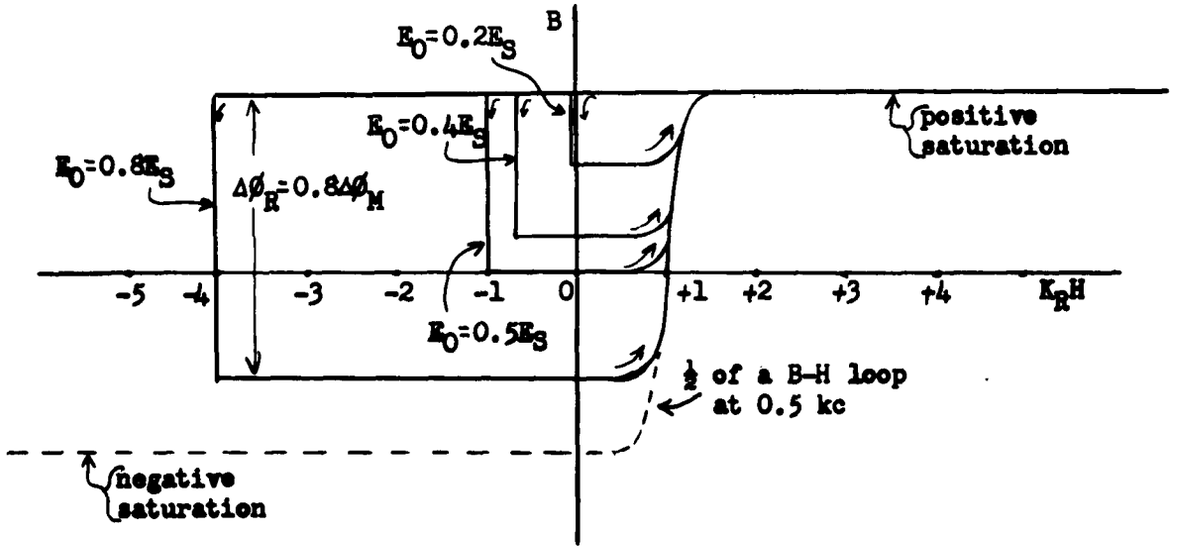


Figure 5.3-22 Theoretical minor B-H hysteresis loops of ST_1 of Figure 5.3-18. Using same assumptions as Figure 5.3-20 and 5.3-21, if stable operation could be obtained.

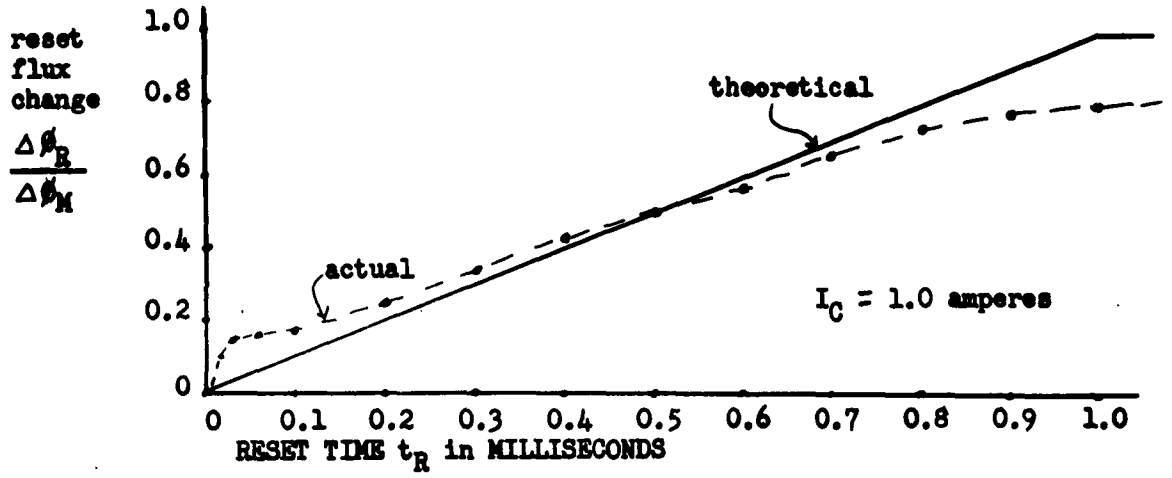


Figure 5.3-23 Flux reset as reset time t_R varies with control current constant. The theoretical characteristic is compared to the actual. $\Delta\phi_R$ is the flux change from positive saturation that occurs while Q_1 is turned off. $\Delta\phi_M$ is the maximum available flux change which is from positive to negative saturation.

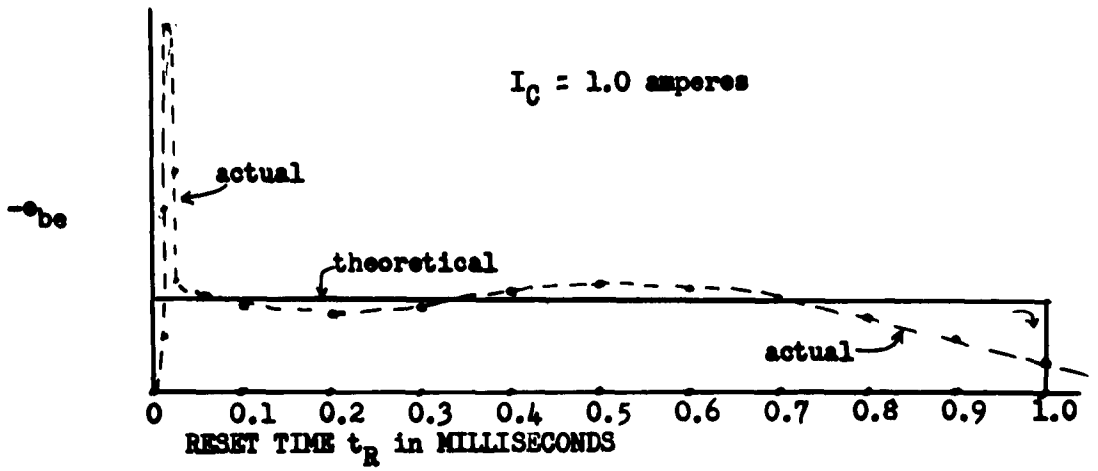


Figure 5.3-24 Induced voltage in a winding of ST_1 during flux reset as reset time t_R varies. During reset Q_1 is turned off and the primary and secondary winding of Q_1 are effectively open circuit. The high peak of $-e_{be}$ results from the flux change in the core of ST_1 as it drops out of positive saturation.

No. Cycle =	0	1	2	3	4	5	6	7	8	9	10	∞
at I_C =	0.025 amps.											
E_0/E_S	0.20	0.198	0.201	0.200	s t a b l e							0.20
t_R/t_{RM}	0.78	0.802	0.799	0.800								0.80
at I_C =	0.667 amps.											
E_0/E_S	0.40	0.364	0.424	0.391	0.405	0.396	0.403	0.398	0.401	0.399	0.400	0.40
t_R/t_{RM}	0.56	0.636	0.576	0.609	0.595	0.604	0.597	0.602	0.599	0.600	0.600	0.60
at I_C =	1.0 amps.											
E_0/E_S	0.50	0.45	0.550	0.45	0.55	0.45	n e v e r r e t u r n t o					
t_R/t_{RM}	0.45	0.55	0.450	0.55	0.45	0.55	E_0/E_S = 0.5 or t_R/t_{RM} = 0.5					
at I_C =	1.5 amps.											
E_0/E_S	0.60	0.54	0.69	0.465	0.748	0.377	0.935	0.037	1.000	0.000	1.000	
t_R/t_{RM}	0.36	0.46	0.31	0.535	0.252	0.623	0.065	0.943	0.000	1.000	0.000	
at I_C =	4.0 amps.											
E_0/E_S	0.80	0.48	1.000	0.000	1.000	n o t s t a b l e						
t_R/t_{RM}	0.12	0.52	0.000	1.000	0.000							

Figure 5.3-25 Table showing recovery or instability for various settings of I_C. During cycle number zero, the reset time t_R is disturbed by a 10% reduction.

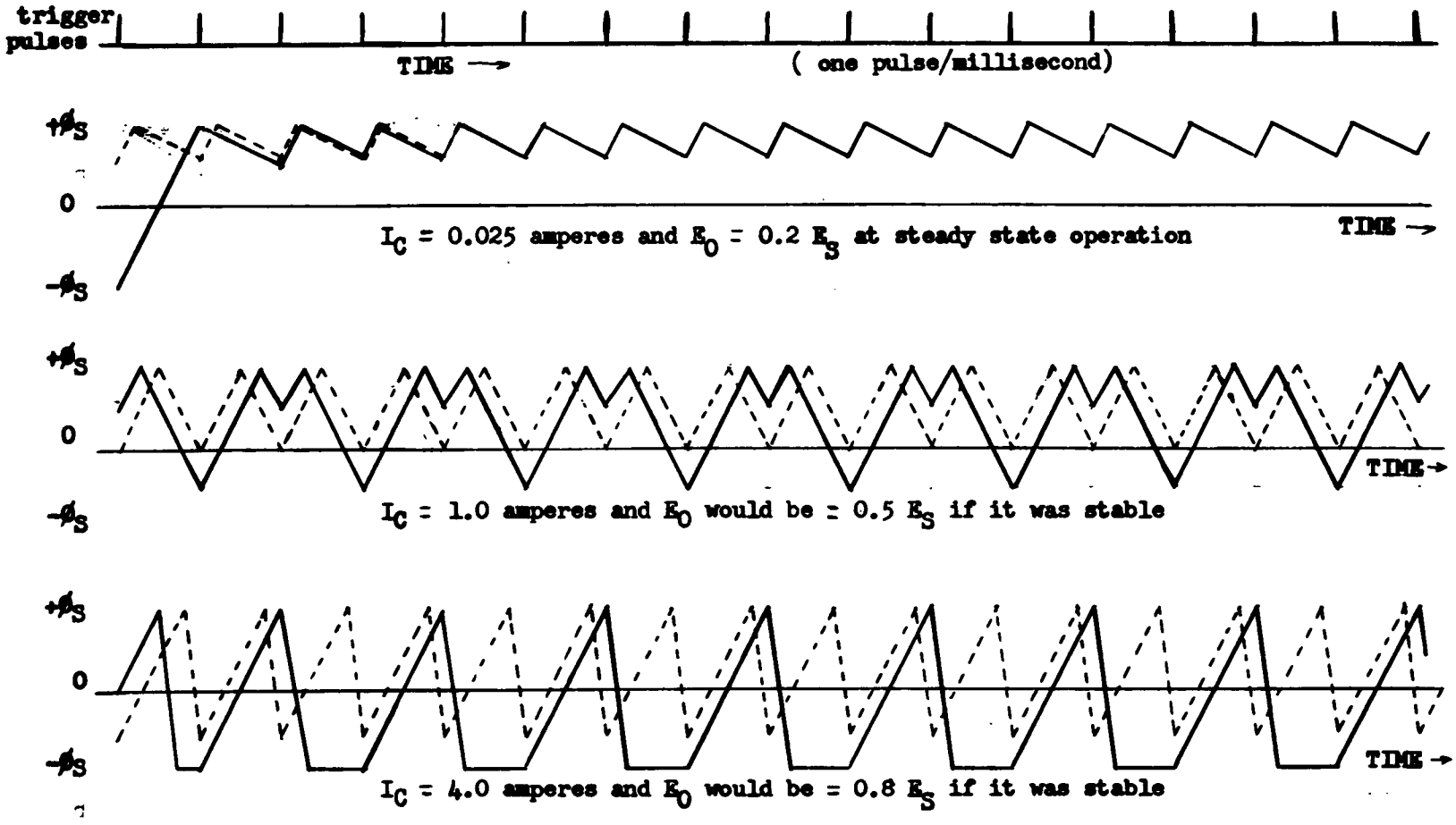


Figure 5.3-26 Flux position of ST_1 core vs time showing transition of recovery to $E_0 = 0.2\ E_S$ after t_R is disturved and instability that results after E_0 is disturbed from $E_0 = 0.5\ E_S$ or $E_0 = 0.8\ E_S$. Solid curves of ϕ after disturbance and dotted curve of ϕ if not disturbed.

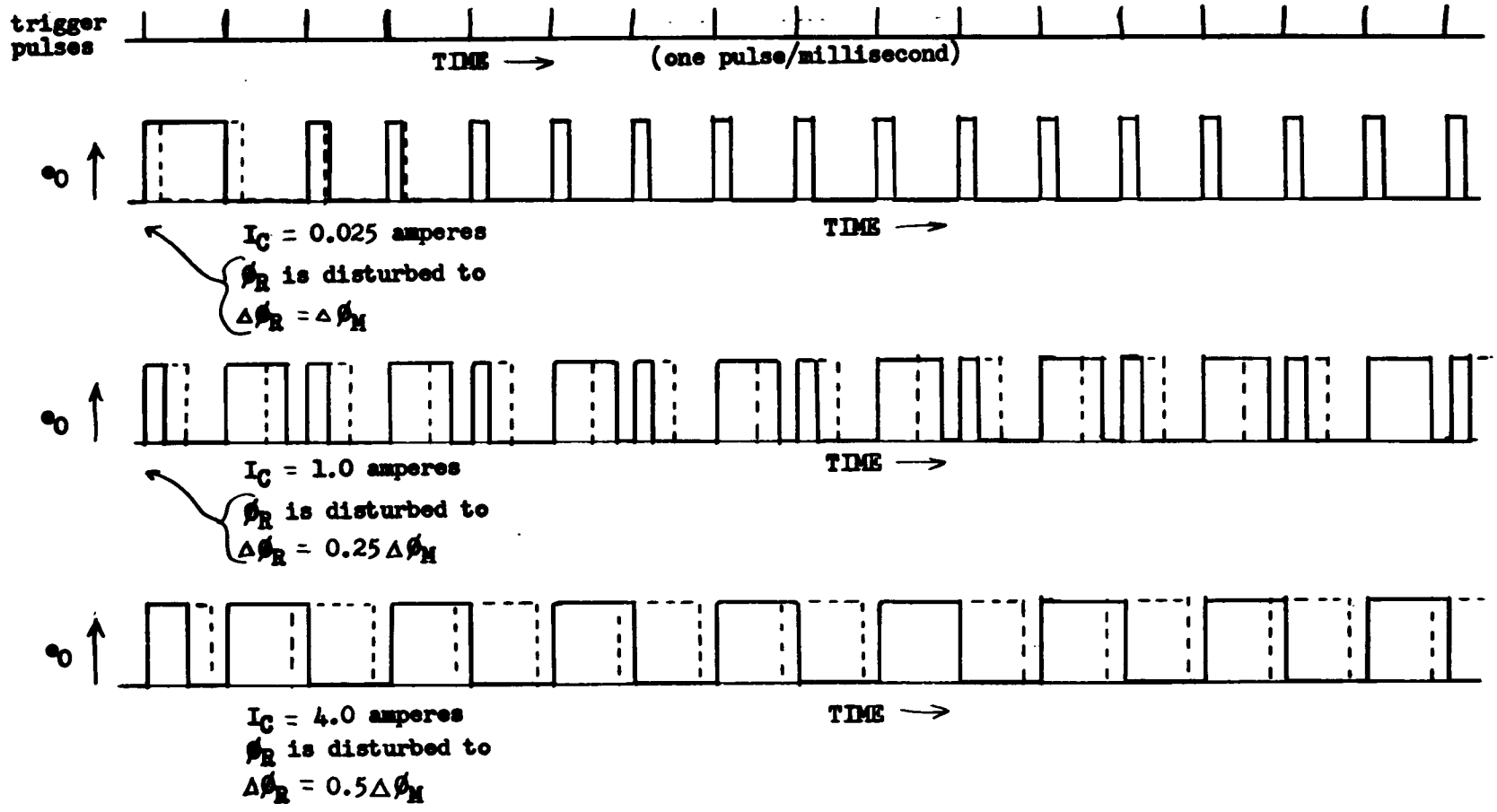


Figure 5.3-27 Waveforms of voltage e_0 (Figure 5.3-18) corresponding to ϕ waveforms of Figure 5.3-26. Solid curves show recovery or instability of instantaneous output voltage e_0 of Figure 5.3-18.

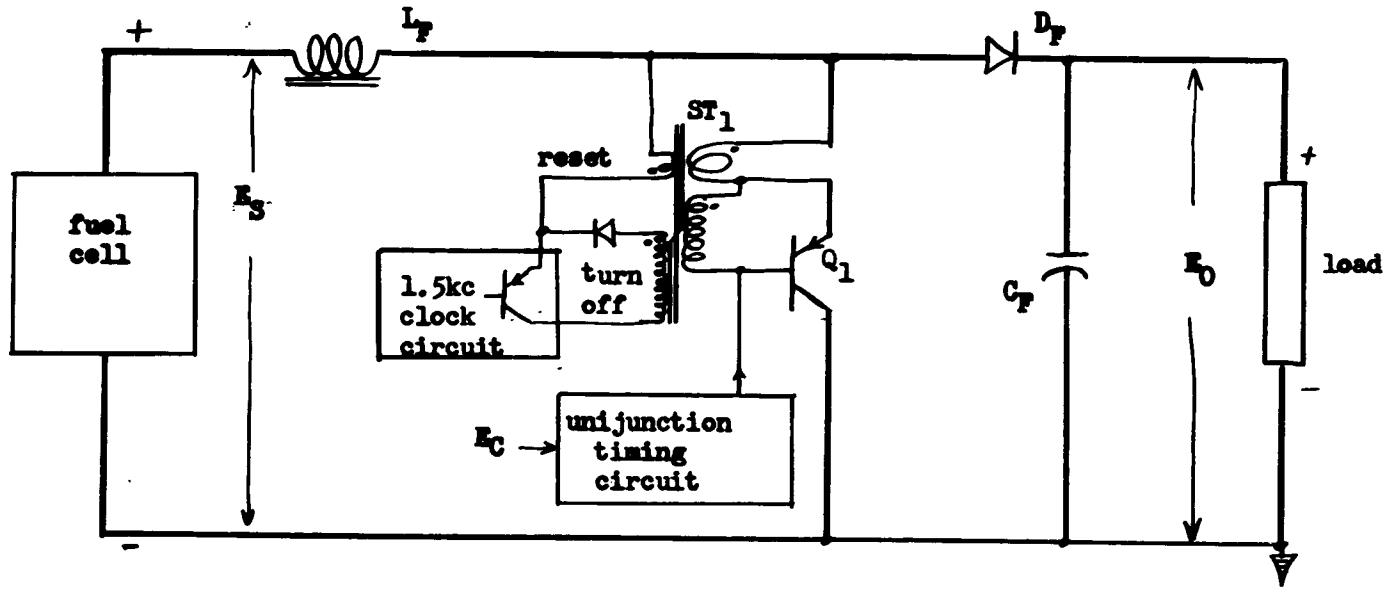


Figure 5.3-28 Basic circuit for control circuit #2. The power is controlled by Q_1, L_F and D_F in the same manner as used in control circuit #1, described earlier in this report. A clock circuit turns off Q_1 by a new technique using ST_1 and the clock circuit resets ST_1. The unijunction timing circuit turns on Q_1 after a delayed period of time t_D after the clock circuit resets ST_1. The time t_D is a function of the control voltage E_C and output voltage E_O can be controlled by E_C from $E_O = E_S$ to $E_O \cong 4\ E_S$.

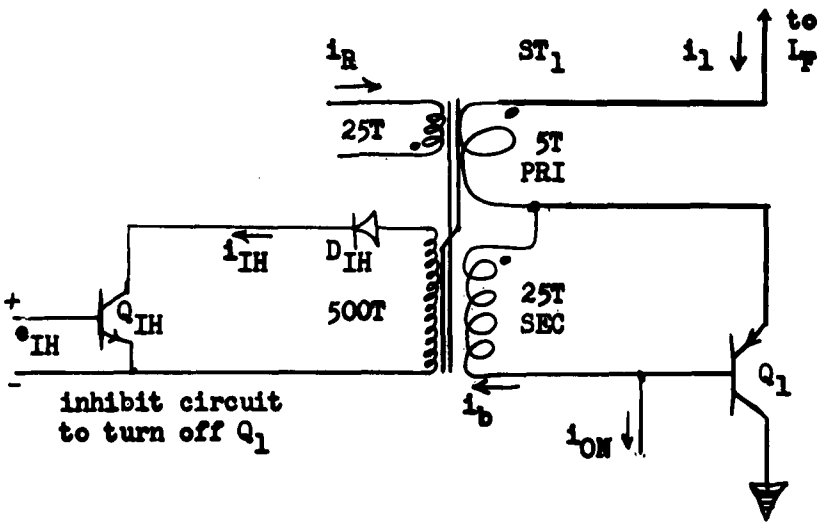


Figure 5.3-29 The operation of the power transistor Q_1 is illustrated by the use of i_{ON}, i_{IH} and i_R. Transistor Q_1 is turned on by i_{ON} as i_{ON} is applied for 10 microseconds. Q_1 is turned off by the inhibit circuit of Q_{IH} and ST_1. When Q_{IH} is turned on, the base drive current i_b is inhibited from Q_1 and Q_1 turns off. After Q_1 turns off reset current i_R resets ST_1. The number of turns of ST_1 illustrates a typical turns ratio of winding and not final design data.

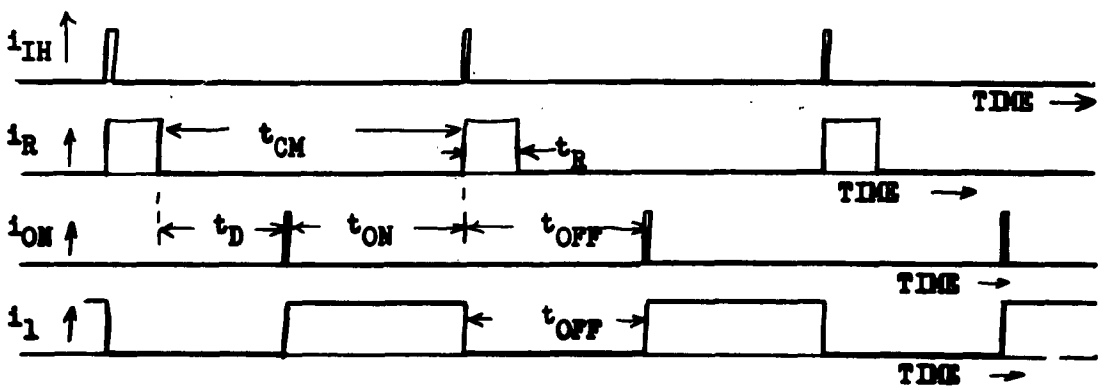


Figure 5.3-30 Wave shapes and phase relation of current that operate Q_1 and ST_1 of Figure 5.3-29. The frequency is 1.5 KC, i_{IH} flows for about 20μS, i_R for 100μS, i_{ON} for 10μS, and i, for time t_{ON} time t_{ON} is controlled from $t_{ON} = 0$ to $t_{ON} = t_{CM}$.

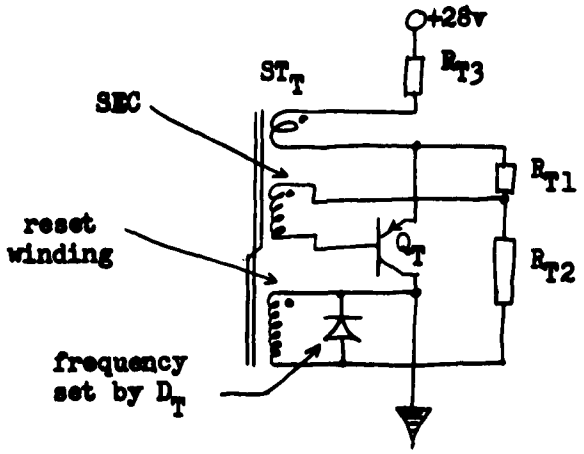


Figure 5.3-31 Clock circuit using a saturable transformer transistor oscillator as described in Reference 2. Q_T is "on" for approximately 100μS and "off" for 600μS. The time Q_T is off is set by timing diode D_T. During reset of ST_T the voltage of the reset winding is limited by the forward voltage drop of D_T. ST_1 is designed for the flux to reset from positive to negative saturation level in 600μS (± 10%) when limited by D_T.

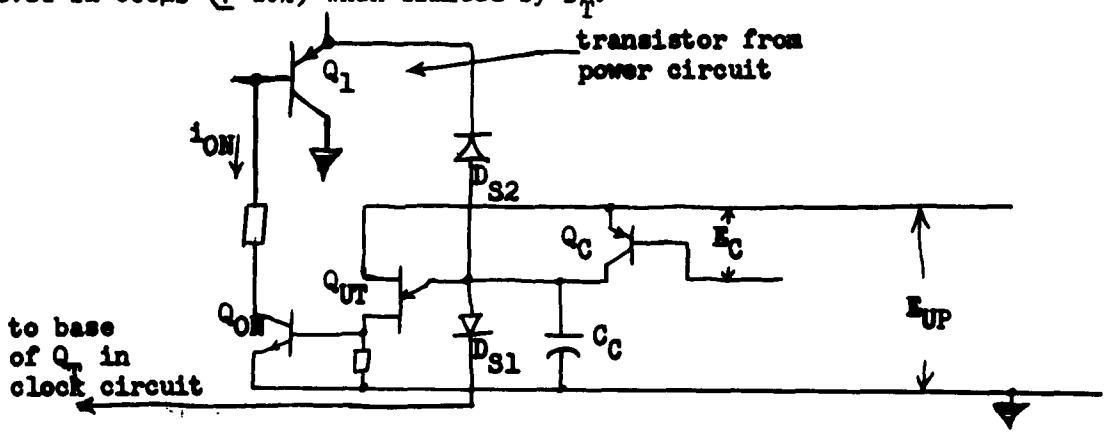


Figure 5.3-32 Unijunction timing control (UTC) for controlling the interval of time between the time ST_1 is reset and Q_1 is turned on. If D_{S1} and D_{S2} were removed, the UTC would oscillate as a function of the resistance (R_{Ce}) of Q_C. Diodes D_{S1} and D_{S2} inhibits the oscillation and UTC provides a timing circuit that starts when D_{S1} blocks current and stops when Q_1 is turned on by Q_{ON} and Q_{UT}. The UTC provides a delay time t_D for turning on Q_1 after ST_1 (Figure 5.3-29) is reset. Time t_D is controlled by E_C.

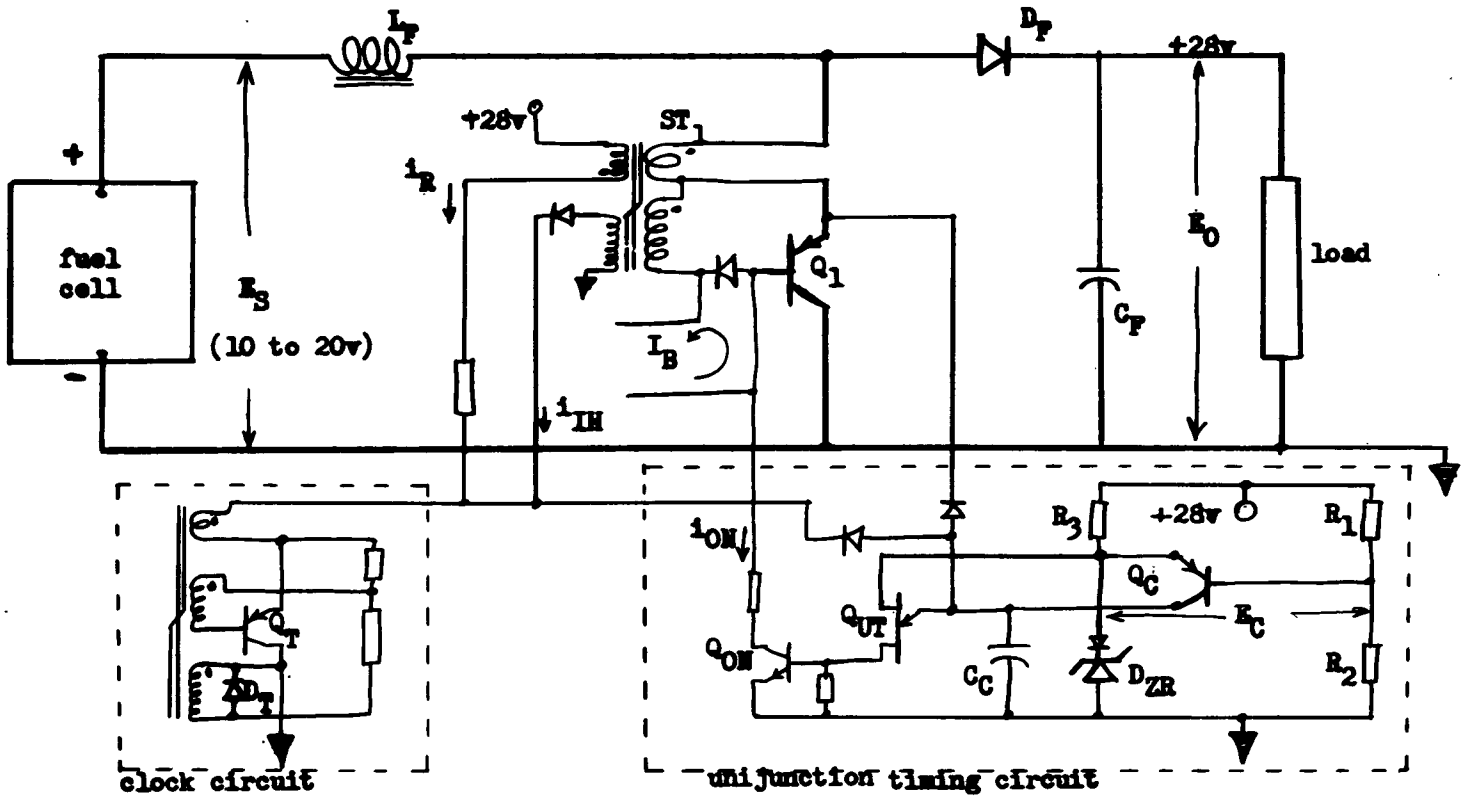


Figure 5.3-33 Control circuit #2 with the power circuit, clock, and unijunction timing control. Bias $I_B \cong 50$ ma, is supplied from clock or separate current source. Zener reference bridge D_{ZR}, R_1, R_2 and R_3 measure E_0 and supply E_C to control Q_1 and regulate E_0. Diode in series with D_{ZR} provides temperature compensation for Q_C.

5.4 High Frequency Switching Investigation

5.4.1 Introduction

The purpose of and approach to the high frequency switching investigation was summarized in Section 5.2.3. As indicated, the intent of this investigation is to establish methods of achieving efficient circuits with higher operating frequencies than presently used. Higher operating frequencies result in smaller, lighter voltage conversion circuits due to the reduced magnetic and dielectric component sizes. Unfortunately, losses tend to increase with operating frequency. The use of powdered iron core transformers, ferrite core transformers, high speed switching power transistors, and fast recovery diodes will be examined in order to minimize these losses.

A thorough understanding of the effects of operating frequency on component operation and losses is essential first requirement to designing efficient circuits with higher operating frequencies. This study was begun with a thorough investigation of the fundamental behaviour of power transformer. The following paragraphs summarize this power transformer examination and give the pertinent conclusions.

5.4.2 Summary of Power Transformer Investigation

The power transformer is one of the major components in a transistor voltage converter circuits, both from the standpoint of weight and losses. Although presumably well understood, the design of a transformer becomes progressively more difficult as one employs higher and higher frequencies. A weight advantage is realized at higher frequencies; however, this advantage is offset somewhat by the more predominant effects of core losses, skin effect in conductors, distributed winding capacitances, etc. Therefore, in order to explore the advantage of higher frequency on the weight and efficiency of transformers it is necessary to reconstruct some of the elementary design understanding.

Design Parameters

Consider, for example, a small power transformer operating at a relatively low power frequency such as 60 cycles per second. Therefore, skin and eddy current effects will be small. It will be assumed that the transformer is of simple construction consisting of a common tape wound iron structure on which are located primary and secondary windings. Electrical coupling between windings will be considered good. The core will, however, exhibit hysteresis loss and will become saturated when sufficiently excited.

The windings are of copper and have resistance and losses. Thus, while the transformer is simplified, it is not ideal, in the sense that it does have losses and some limitations such as saturation. Other limitations will be introduced later.

Now assume sinusoidal excitation of one of the transformer windings. Let this be sufficient to drive the core symmetrically about the origin of its B-H core characteristic, although not necessarily into saturation. The voltage, frequency and core flux are related as follows:

(5.4-1) $$E_M = \sqrt{2}E = \omega N A_c B$$

where

E_M is the peak amplitude (not r.m.s.) of the sinusoidal exciting voltage

E is the r.m.s. amplitude of the voltage

ω is the angular frequency expressed in radians per second

N is the turns of the winding under excitation

A_c is the core cross section which is assumed to be uniformly excited.

B is the peak amplitude to which the magnetic core flux density is driven. It is not necessarily the saturation level but some intermediate level where linearity is achieved.

The core depends primarily upon the exciting voltage for its sinusoidal swing in flux density. However, some exciting current is required and this is related to the coercive force of the core material by the relation:

(5.4-2) $$I_x = \frac{\ell_c H_c}{N}$$

where I_x is the exciting current

ℓ_c is the core length of the average path

N is the turns of the winding previously reffered to

H_c is the coercive force of the magnetic field. The magnitude of H_c increases with frequency, a fact which will be elaborated upon at a later point.

The core loss is then determined by integrating the product of the instantaneous sinusoidal voltage and exciting current over one cycle. For a square loop type material, the exciting current is approximately a square wave. In an alternate approach, the core loss is obtained by the product of frequency and the closed integral around the particular hysteresis loop traversed. By either method, the core loss is given by the relation:

(5.4-3) $$P_c = \left(\frac{2}{\pi} E_M\right)(I_x) = \frac{2}{\pi} \omega(A_c \ell_c) BH$$

Thus, the core loss is rather simply related to the core volume and to the flux density and magnetic field strength. Because H_c increases with frequency, the core losses for a fixed size increase more than directly with frequency.

In an efficient design the window of the transformer will be entirely filled with conductors except for space needed for insulation, etc. The wire cross section, number of turns, and window size may be related using a simple winding factor in the following manner.

(5.4-4) $$A_W = Zk N A_o$$

where

A_W is the area of the transformer core window

k is the winding factor -about 2.5 for common small transformers

N is the turns per winding

A_o is the wire conducting cross section

An equal allotment of space is provided for both windings as represented by the factor of Z in Equation 5.4-4.

The transformer primary and secondary load current is presumably many times that of the previously considered core exciting current. It is the product of the wire conducting cross section and the current density:

(5.4-5) $$I = J A_o = \frac{J A_W}{2kN}$$

where

I is the load current

J is the current density

The voltage drop in each of the windings results from winding resistance which is a function of the resistivity of the wire, the wire cross section, and the number of turns, and the mean length of turn. This latter quantity like the core cross section, the core flux path, and the window area can be calculated entirely from the core geometry. The voltage drop for one winding is given by:

(5.4-6) $$E_R = R_W \times I = \left(\sigma \frac{\ell_M N}{A_o}\right) (J A_o)$$

where

E_R is the voltage drop resulting from winding resistance

R_W is the winding resistance

σ is the resistivity of the wire

ℓ_M is the mean length of turn

The winding losses for both primary and secondary based upon equal allotments of window cross section and identical mean lengths of path are given by:

$$(5.4\text{-}7) \qquad P_W = 2\,E_R\,I$$

$$= 2\,(\sigma J \ell_M N)\,(J\,A_o)$$

If Equation 5.4-4 is substituted for the wire cross section, the total winding losses become:

$$(5.4\text{-}8) \qquad P_W = I \times E_R = \frac{\sigma}{k}\,(A_W\,\ell_M)\;J^2$$

As the core losses in Equation 5.4-3 were related to the core volume, the winding losses in Equation 5.4-8 are related to the winding volume; both volumes determined from the core geometry.

The transformer rating is based upon the voltage needed for excitation and the load current which it handles. Thus, from equations 5.4-1 and 5.4-5 the rated load power is given by:

$$(5.4\text{-}9) \qquad P_o = E \times I$$

$$= (\omega\,N\,A_c\,B)\left(\frac{J\,A_w}{2\,k\,N}\right)$$

$$= \frac{\omega}{2\,k}\,(A_c\,A_w)\,B\,J$$

The transformer power rating is determined again by the core geometry as well as the frequency and the current and flux densities. In Equation 5.4-9 no allowance was made for power factor. The more general case would include a term for power factor.

Whereas the transformer losses depend upon the third power of the transformer geometry, the power rating depends upon the fourth power. Larger transformers are more efficient since the power rating increases more rapidly with increased size than do the losses. The power rating of a given size transformer increases directly with frequency; however, the core loss increases more rapidly so that derating becomes progressively necessary at higher frequencies.

Efficiency

The efficiency of a transformer is an important measure of its suitability in a power application. Equations 5.4-3, 5.4-8, and 5.4-9 may be substituted into the following expression for efficiency:

(5.4-10) $$\eta = \frac{P_o}{P_o + P_c + P_W}$$

where

η is the transformer efficiency

(5.4-3) $$P_c = \frac{2}{\pi} \omega (A_c \ell_c) B H$$

(5.4-8) $$P_W = \frac{\sigma}{k} (A_W \ell_M) J^2$$

(5.4-9) $$P_o = \frac{\omega}{2k} (A_c A_W) B J$$

It can be shown from the above expressions that at a current density which yields peak efficiency the winding losses equal the core loss. On this basis the rated current density may be calculated from a predetermined core size. If the transformer is operated at half load current, the efficiency becomes:

(5.4-10) $$\eta = \frac{\frac{P_o}{2}}{\frac{P_o}{2} + P_c + \frac{P_W}{4}} = \frac{P_o}{P_o + 2P_c + \frac{P_W}{2}}$$

or at double load current

(5.4-11) $$\eta = \frac{2P_o}{2P_o + P_c + 4P_W} = \frac{P_o}{P_o + \frac{P_c}{2} + 2P_W}$$

In both cases the efficiency is less than when operated at a condition where the core and winding losses are equal.

Although difficult to do in practice, by operating at reduced core excitation (i.e., at proportionately lower supply voltage) when the load current falls off, the efficiency of the transformer is retained. Thus, at half load current and half excitation, the peak efficiency is the same as for full load or full excitation:

(5.4-12) $$\eta = \frac{\frac{P_o}{4}}{\frac{P_o}{4} + \frac{P_c}{4} + \frac{P_W}{4}} = \frac{P_o}{P_o + P_c + P_W}$$

This conclusion is predicated on the assumption that the magnetic field strength (H) in the core varies directly with the level of operating flux density. Up to the point of core saturation, the above assumption is not particularly bad, as illustrated by the relation between field strength and flux density plotted in Figure 5.4-1. This data was obtained for 12 mil selectron from Arnold Engineering Bulletin SC-107.

From the previous examples several conclusions regarding transformer efficiency become apparent:

1. Peak efficiency occurs when winding and core losses are made equal.

2. Transformer efficiency increases with size.

3. If core excitation and load current are varied together, the transformer efficiency is independent of the level of excitation up to saturation.

4. The only way to higher efficiency is by greater transformer size.

5. Operation at a higher flux density (and load current) will permit greater output for a given transformer but not higher efficiency.

To a first approximation a given transformer may be made to operate at the same efficiency over the full range of load from no load to full load. Were it not for core saturation the flux density and current density could be increased together almost indefinitely. The losses and the output would increase together always at the same efficiency, and thereby yield enormous power for a particular size transformer. Some other limitation would be needed to limit the output, such as the Currie Point temperature, melting point of copper, etc.

On the other hand, since transformer efficiency is related to core size and not to the level of output a purely academic approach to achieving a very high transformer efficiency for a requirement involving even a modest power output would be to employ a large structure under-excited and loaded as needed.

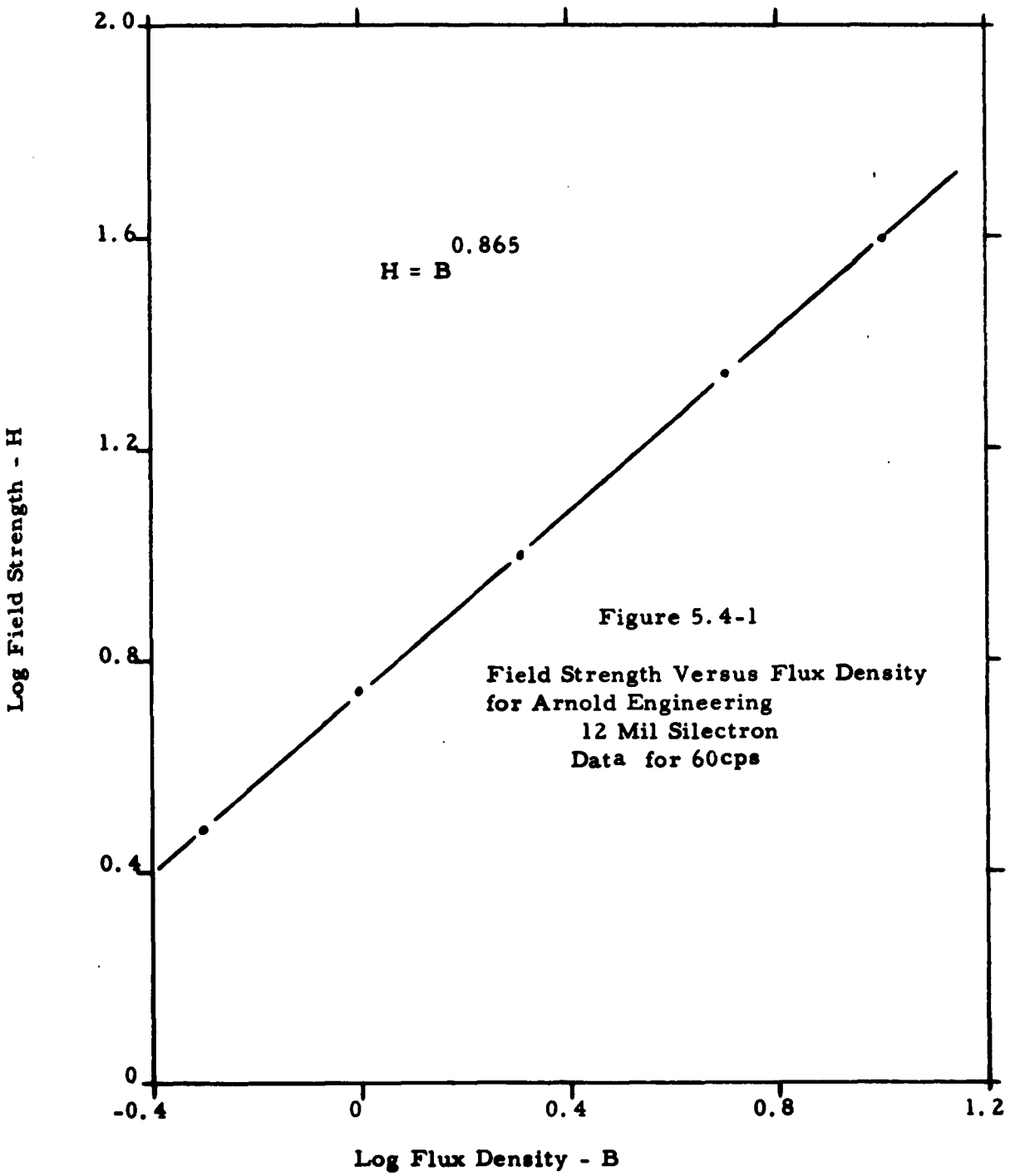


Figure 5.4-1

Field Strength Versus Flux Density
for Arnold Engineering
12 Mil Silectron
Data for 60cps

There are situations where a transformer will be operated under light load a part of the time and where it is totally impractical to reduce excitation. Under these conditions the so-called "All Day Efficiency" may be derived. Here the winding losses are integrated over a period of time where a repeatable pattern has established itself; for example, in the demands upon a power station over a period of a day. These integrated losses are then equated to the steady loss in the core excitation as a basis for design of the transformer. The peak efficiency is in this manner located somewhere between minimum and maximum load values. On a similar basis the space allotment for windings of a transformer will be divided according to the expected loading. In the present transformer the secondary winding handles the same load as the primary winding except for the losses of the transformer. Therefore an equal window space and volume allotment is provided for both windings. However, in a transformer where the windings are not equally loaded as in full wave rectification achieved from a center tapped secondary winding, the space allotment would be 41% of the total window area for the primary and the remainder for the secondary. The primary winding loss would also be 41% of the total winding loss, the remaining loss divided between the two halves of the secondary winding. Losses between windings are not necessarily the same when operating at peak efficiency of the transformer.

Transformer Weight

While the consideration of efficiency is extremely important, the design of a transformer must be based upon other important considerations. Even in a large power installation a line must be drawn somewhere on a physical size. Increasingly large structures, though more efficient, are of little value if the initial cost exceeds the savings from higher efficiency. Few transformers are designed to operate under-excited for sake of higher efficiency in large physical size. Where a size or weight limitation is imposed the reverse may be true. As an example, consider a particular transformer operated at its maximum value of flux density. Peak efficiency results from operating this transformer at a load where winding and core losses are equal. However, the efficiency is not seriously reduced by increasing the load current to double its value at peak efficiency. Although the winding losses quadruple, the core losses remain the same, so that the total losses are only slightly more than double. The power output is doubled so that with only a slight sacrifice in efficiency the transformer rating has been doubled with no increase in physical size.

Where transformer weight becomes a factor in overall performance it is seen that a definite advantage is realized by operating the transformer with winding losses in excess of core loss. A criterion is needed to establish the proper ratio between the two loss components so as to achieve maximum capability in both efficiency and physical size.

If the required power output or rating of a proposed transformer has already been established, this quantity becomes a constant in the Equation (5.4-10) for efficiency. From the fixed power rating, the current density may be expressed in terms of the proposed core geometry and power rating by means of Equation 5.4-9. Using this to eliminate current density the expression for efficiency becomes:

$$\eta = \frac{1}{1 + aD^3 + \frac{b}{D^5}} \tag{5.4-13}$$

where

D is a critical dimension of cores of similar construction (for example, the diameter of a torroid).

P_o is constant, thus

$$\frac{P_c}{P_o} = \left(\frac{2\omega BH}{\pi P_o}\right) A_c \ell_c = aD^3 \tag{5.4-14}$$

$$\frac{P_W}{P_o} = \left(\frac{4k\sigma P_o}{\omega^2 B^2}\right) \frac{\ell_M}{A_c^2 A_W} = \frac{b}{D^5} \tag{5.4-15}$$

and the values of coefficients a and b depend upon core dimensional relations as yet undetermined. The nature of Equation 5.4-13 illustrates that maximum efficiency based upon a fixed power rating will occur where the losses are in the following relation:

$$P_W = \frac{3}{5} P_c \tag{5.4-16}$$

Thus, the winding losses would be less than the core loss, a conclusion which disagrees with that previously suggested. However, this conclusion given by Equation 5.4-16 is based upon a transformer of fixed power rating where size is allowed to vary. This is the usual case in design. The previous conclusion of Equation 5.4-10 was based upon a transformer of fixed size, but the power output was allowed to vary.

Many approaches to transformer optimization are possible. One such approach which factors in both weight and efficiency is that of designing a transformer to achieve a minimum loss weight product. In this case, it can be shown that minimum loss weight product occurs when:

(5.4-17) $$P_W = 3P_c$$

This result is in agreement with the previous conclusion proposing an increased current rating beyond that which would constitute equal loss components, so as to step up the transformer rating without additional weight. With the winding loss three times that for peak efficiency the output would be up by 72% and the total losses up by 100%. An added advantage occurs for operation under less than rated load in that the efficiency is retained over a more significant portion of the total load variation. No simple relation between weight and efficiency or transformer loss will satisfy the general case. One must be guided by a certain judgement involving the makeup of the system and the mission to be performed.

Core Dimensions

Although the transformer may have any one of several core configurations, only one is presently considered. This is that of a toroidal core with rectangular cross section. Primary and secondary windings are each wound uniformly distributed about the core, one on top of the other. This core configuration is indicated in Figure 5.4-2. First consideration will be given to the relation between dimensions which will yield maximum power out of a given weight of transformer. Equation 5.4-9 shows the output to be proportional to the product of core and window cross sections. In effect, these cross sections are to be maximized for the volumes they represent. Other criteria which might be employed to prescribe dimensional relations of the core are those of minimum flux leakage, distributed capacitance, etc. These quantities are however given secondary consideration for the present.

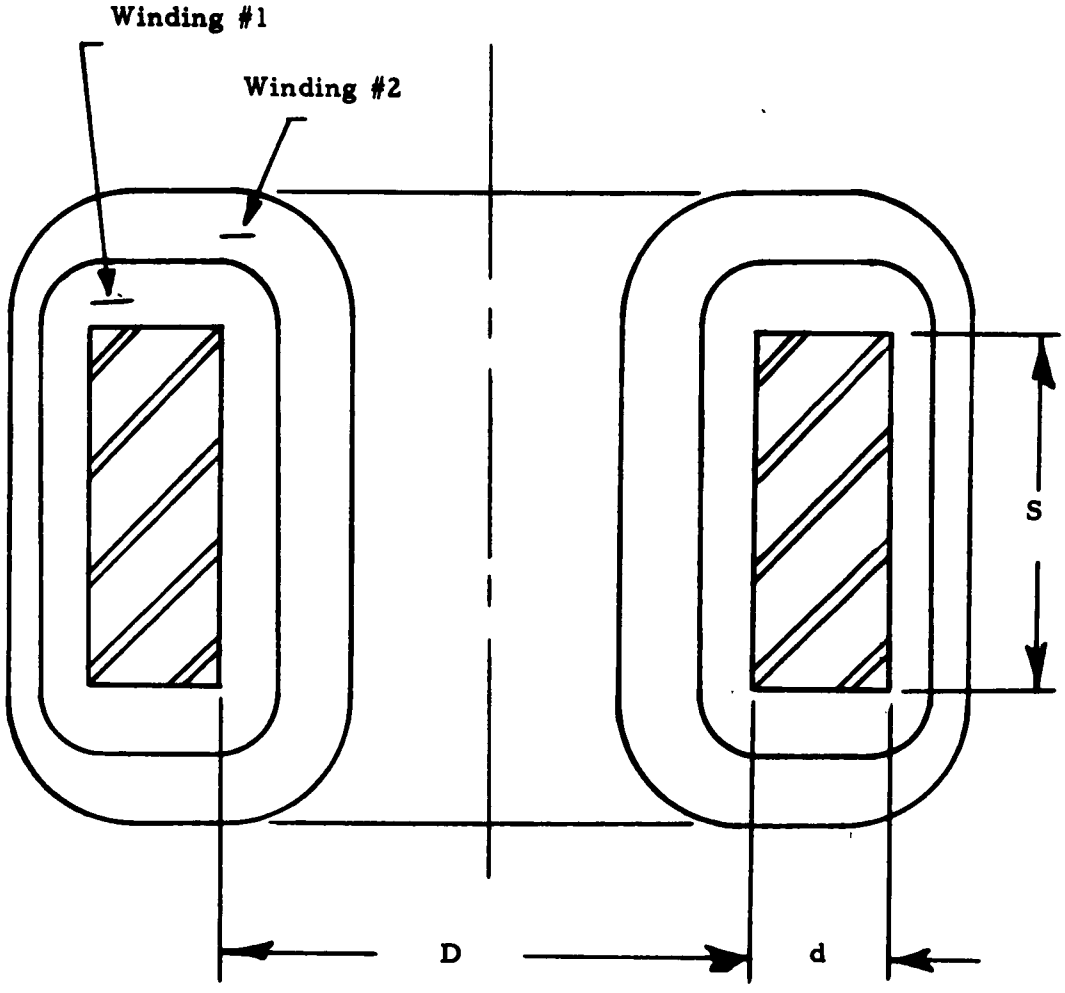


Figure 5.4-2 Toroidal Core Configuration

Neglecting the weight of mounting brackets, lead wires or terminals, and other intangibles, the optimum core dimensions may be determined from expressions already derived. First, let the performance ratio be determined. This quantity is arbitrarily defined as the third power of the transformer output to the fourth power of the transformer weight. It depends upon the interrelation between transformer dimensions but not upon overall size:

$$(5.4\text{-}18) \qquad y = \frac{P_o^3}{M^4} = \frac{\left[\frac{\omega}{2k}(A_c A_W) B J\right]^3}{\left[\delta_c A_c \ell_c + \delta_W A_W \ell_M\right]^4}$$

where

y is the performance ratio

δ_c is the effective core density including reduced spacing of laminations or powder.

δ_W is the effective winding density and also allows for insulation and spacing.

M is the total weight of transformer core and windings.

As previously noted the current density depends upon the relation between core loss and winding losses. For purposes of generality let this relation be expressed by the proportionality constant ϑ :

$$(5.4\text{-}19) \qquad P_W = \vartheta P_c$$

ϑ may have a value anywhere from 3/5 to 3 depending on the nature of the transformer application. Substituting Equations 5.4-3 and 5.4-8 into Equation 5.4-19 and solving for the current density:

$$(5.4\text{-}20) \qquad J = \sqrt{\left(\frac{2\vartheta k \omega B H}{\pi p}\right) \frac{A_c \ell_c}{A_W \ell_M}}$$

The core geometry from Figure 5.4-2 is expressed by the following relations:

$$(5.4\text{-}21) \qquad A_c = S d = M N D^2$$

(5.4-22) $$A_W = \frac{3\pi}{16} D^2$$

(5.4-23) $$\ell_c = \pi(D + d) = \pi D(1 + m)$$

(5.4.-24) $$\ell_m = 2(s + d + \frac{\pi}{8} D) = 2D\left(\frac{\pi}{8} + m + n\right)$$

where

m and n are dimensionless ratios, defined as follows:

(5.4-25) $$m = \frac{d}{D}$$

(5.4-26) $$n = \frac{S}{D}$$

Upon substituting Equation 5.4-20 through 5.4-26 into Equation 5.4-18 for the performance ratio, one obtains after simplifying:

(5.4-27) $$y^2 = C \frac{(Mn)^9 (1+M)^3}{[MN (1+M) + b (a+M+N)]^8 (a+M+N)^3}$$

where

(5.4-28) $$a = \frac{\pi}{8}$$

(5.4-29) $$b = \frac{3}{8} \times \frac{\delta_W}{\delta_c}$$

(5.4-30) $$c = \frac{\left(\frac{3\pi\delta\omega\bar{B}^3 H}{64kp}\right)^3}{(\pi\delta_c)^8}$$

The optimum values of m and n for maximizing the performance ratio in Equation 5.4-27 are:

$$m = 0.8$$

$$n = 1.7$$

These values are based upon an estimate of 1/4 for b. The specific gravity and space factors of iron, copper, and insulation taken as follows:

Material	Specific Gravity	Space Factor	Product
Copper	9	0.4	3.6
Insulation	2	0.6	1.2
Iron	8	0.9	7.2

Thus:

$$b = \frac{3}{8} \times \frac{3.6 + 1.2}{7.2} = \frac{1}{4}$$

For other values of b the optimum ratios of core dimensions follow the curves shown in Figure 5.4-3. The value of n is about double that of m for all values of b. It is gratifying that the core shape for optimum performance depends only upon the ratio of copper and iron effective densities. For the further study of the transformer under the effects of changing frequency, core size, etc., it is desirable to at least maintain the relative shapes.

Effect of Frequency

The contribution of higher frequency in design of the transformer is primarily that of permitting a significant reduction in size for the same power rating. Iron loss, however, tends to become greater as frequency increases. Ultimately, the increased losses make the higher supply frequencies impractical for a particular core material.

In order to examine the effects of frequency on transformer design quantitatively, the core material loss must be known. Figure 5.4-4 shows a plot of core loss versus frequency for 12 mil silectron of Arnold Engineering Company. The core loss varies by nearly the 1.5 power of frequency and the 20 power of B. The power loss and power output expressions may be written as:

$$P_c = a\, A_c \ell_c B^2 \omega^{3/2} \tag{5.4-31}$$

$$P_w = b\, A_w \ell_m J^2 \tag{5.4-32}$$

$$P_o = c\, A_c A_w \omega J B \tag{5.4-33}$$

where

a, b, and c are proportionality constants.

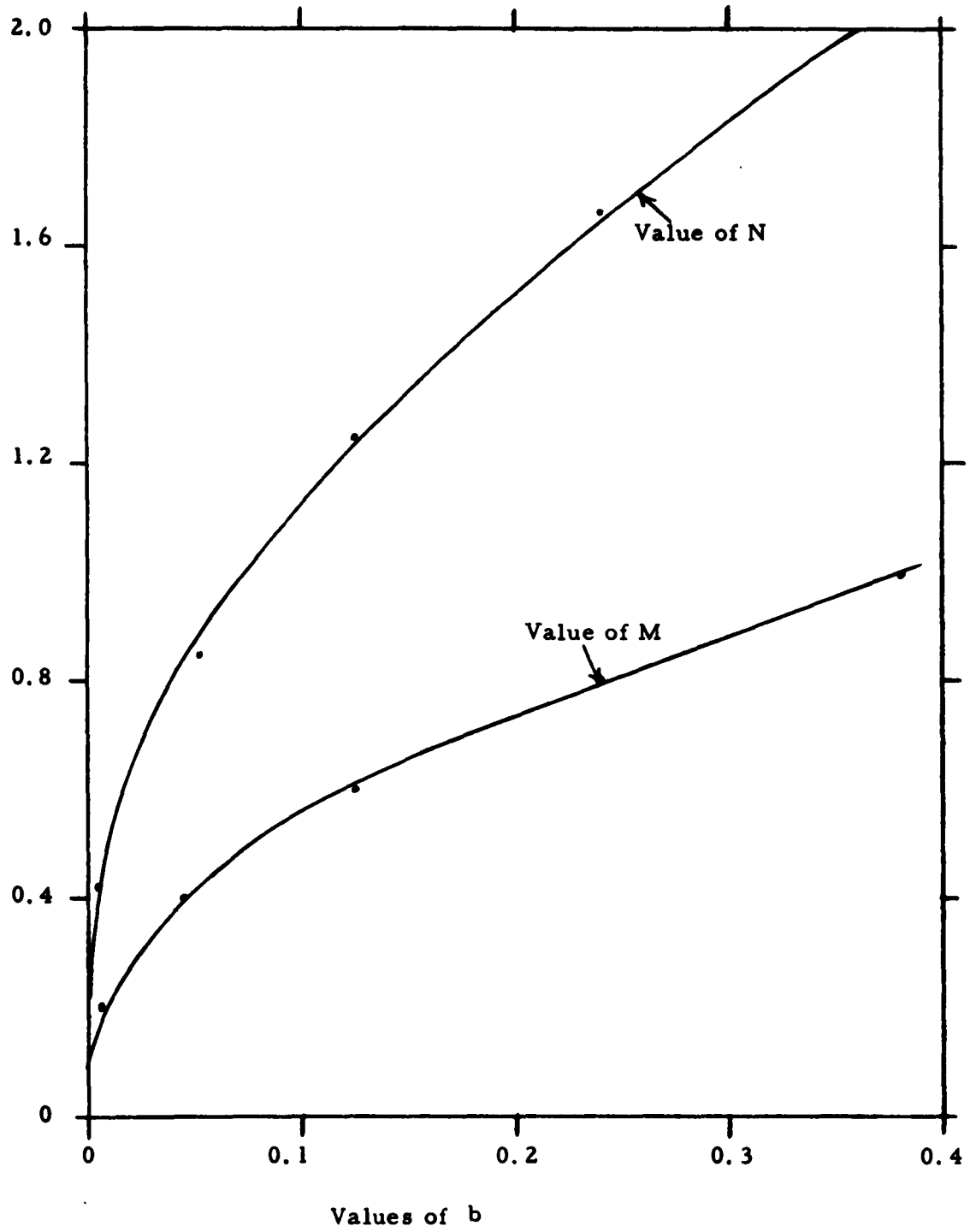


Figure 5.4-3 Value of Dimensionless Ratios Versus Density Ratio

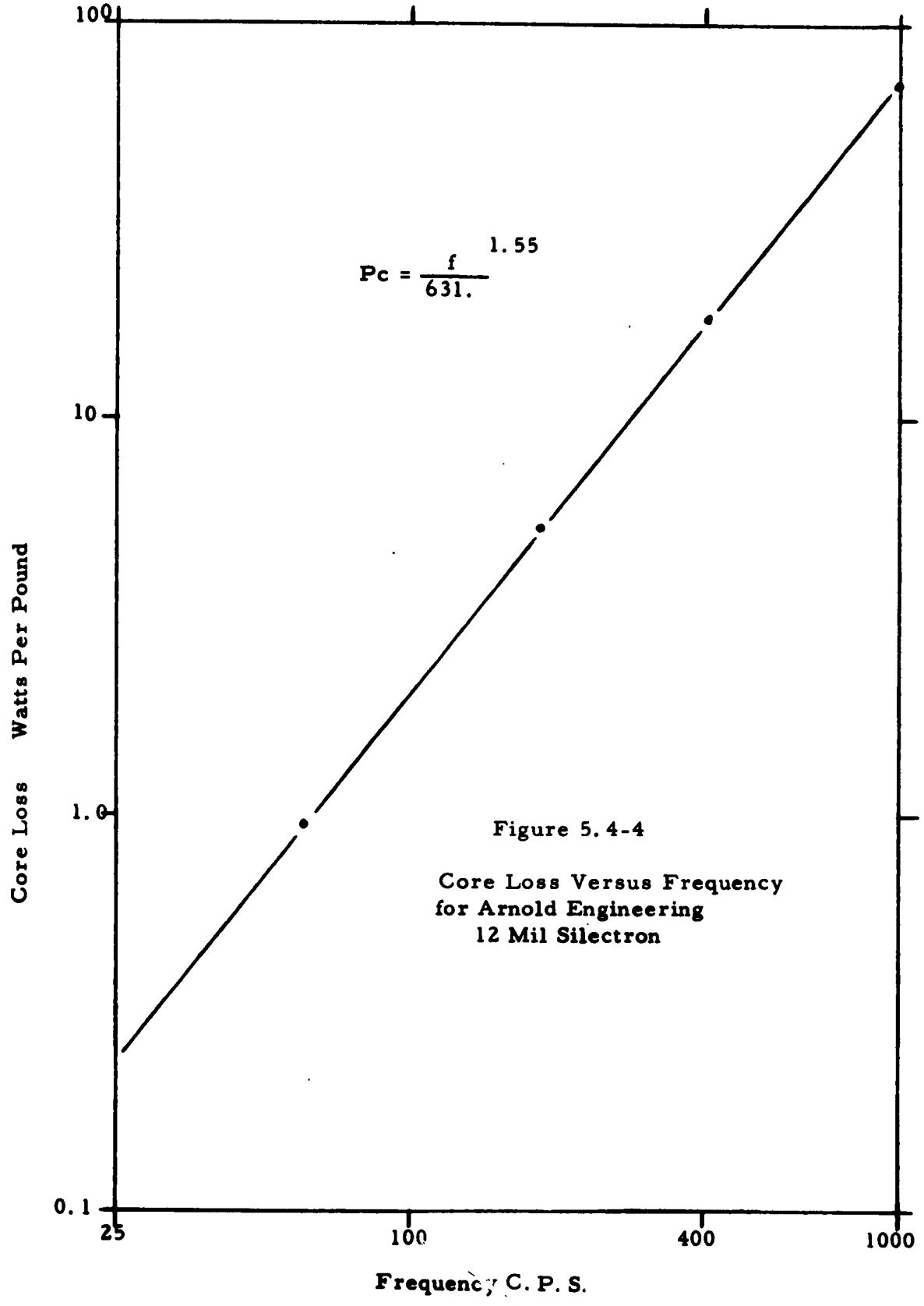


Figure 5.4-4

Core Loss Versus Frequency
for Arnold Engineering
12 Mil Silectron

If a constant relation between core loss and winding loss the current density variation with frequency is:

(5.4-34) $$J = k\,\omega^{3/4}$$

The relation between core and winding volumes is constant assuming that the material densities remain the same through the frequency range. The power output for a particular transformer of the above silectron will vary with frequency as follows:

(5.4-35) $$P_o \propto \omega^{7/4}$$

And the efficiency of the same transformer will vary with frequency according to:

(5.4-36) $$\eta = \frac{1}{1 + d\,\omega^{-1/4}}$$

where

d is a constant of proportionality

The above improvement of efficiency with higher frequency is for a particular transformer and therefore provides no reduction in weight at higher frequencies. A transformer designed to operate at the higher frequency with the same power rating will be reduced in size, the critical dimension depending on frequency from Equation 5.4-33 as follows:

(5.4-37) $$D \approx w^{-7/16}$$

Under this condition of reduced size, the power loss components for delivering the same power output will vary according to:

(5.4-38) $$P_w = \delta P_c \approx \omega^{3/16}$$

The efficiency will be less under the same design condition than for the fixed transformer.

(5.3-39)

$$\eta = \frac{1}{1 + d\,w^{3/16}}$$

The product of power loss and weight will vary according to the following relation:

$$(5.3\text{-}40) \qquad (P_c + P_w)M \approx \omega^{-9/8}$$

The ability of a transformer to dissipate the heat of its power losses to its surroundings depends upon the surface area of the transformer and the temperature rise, according to the relation

$$(5.3\text{-}41) \qquad (P_c + P_w) = fA_s \Delta T$$

where

f is the thermal convection to the surroundings

A_s is the transformer surface area

ΔT is the temperature rise of the transformer relative to its surroundings.

Transformer designs for each of several frequencies but all of a specific power rating will experience an increasing temperature rise versus frequency of

$$(5.3\text{-}42) \qquad \Delta T \approx \omega^{17/16}$$

When the design becomes temperature limited so that no greater temperature rise is permitted, higher frequency designs using the same core material may have to operate under reduced excitation (i.e. - lower values of flux density). The size is no longer determined solely by the fixed power condition, but additionally by a fixed temperature rise requirement. This added restriction is obtained upon reducing the flux density below saturation. Using this example of temperature limit for leverage, it is of value to explore the effect of reduced flux density on the other transformer parameters as they vary with frequency. Several design approaches are examined as follows:

1. Fixed Size - Fixed Flux Density

2. Fixed Power Output - Fixed Flux Density

3. Fixed Size - Fixed Power Output

4. Fixed Temperature Rise - Fixed Power Output

5. Fixed Efficiency - Fixed Power Output

In order to provide a better means of comparing the various approaches, the parameters have been first derived as sole functions of frequency. The exponents of frequency have then been tabulated in Figure 5.4.5. For example, if the current density were to vary as the fourth power of frequency under a particular design approach the exponent 4 then appears at the appropriate point in the table. It is important to note that this table is based upon 12 Mil silectron with the following simplifications:

1. Field strength varies as 1.5 power of frequency

2. Field strength varies directly with flux density

From the table, it is apparent that as frequency increases the design which yields the least product of transformer losses and weight, occurs for maximum flux density operation (Column 2). This confirms previous conclusions. On the other hand, the losses increase with frequency for this approach, so that it becomes less efficient. Furthermore, the temperature rise also rises rapidly with higher frequency designs for this approach. A fixed efficiency approach, last column, has much to offer for higher frequency designs. Smaller size and reduced loss weight product are obtained along with only a modest temperature rise. While a fixed size transformer operated at constant output (Column 3) provides increased efficiency and lower temperature rise at higher frequency, it tends to minimize any advantage to higher frequency operation. The improved efficiency, although modest, may be sufficient justification for this approach. Certainly, keeping the transformer size the same reduces design variety.

In succeeding analyses, some of the modifying factors such as skin effect, distributed winding capacitance, etc. will be examined. The incorporation of these effects on the transformer design in a numerical manner may not be easily accomplished. An alternate approach may be more fruitful. This approach would be directed toward using techniques to minimize the disturbing effects, thereby permitting the present analysis to be extended in frequency.

Figure 5.4-5 Exponent Function of Frequency Of Various Parameters Based Upon Fixing Certain Quantities

	Size & Density Fixed	Output & Flux Density Fixed	Size & Output Fixed	Temp Rise & Output Fixed	Efficiency & Output Fixed
Size D	0	$-\frac{7}{16}$	0	$-\frac{1}{12}$	$-\frac{1}{4}$
Flux Density B	0	0	$-\frac{7}{8}$	$-\frac{17}{24}$	$-\frac{3}{8}$
Current Density T	$\frac{3}{4}$	$\frac{3}{4}$	$-\frac{1}{8}$	$\frac{1}{24}$	$\frac{3}{8}$
Power Loss (P_c+P_w)	$\frac{3}{2}$	$\frac{3}{16}$	$-\frac{1}{4}$	$-\frac{1}{6}$	0
Power Output P_o	$\frac{7}{4}$	0	0	0	0
Efficiency η	$\frac{1}{1+a\omega^{-\frac{1}{4}}}$	$\frac{1}{1+a\omega^{\frac{3}{16}}}$	$\frac{1}{1+a\omega^{\frac{1}{4}}}$	$\frac{1}{1+a\omega^{-\frac{1}{6}}}$	$\frac{1}{1+a}$
Loss x Weight (P_c+P_w) M	$\frac{3}{2}$	$-\frac{9}{8}$	$-\frac{1}{4}$	$-\frac{5}{12}$	$-\frac{3}{4}$
Temp Rise ΔT	$\frac{3}{2}$	$\frac{17}{16}$	$-\frac{1}{4}$	0	$\frac{1}{2}$

5.5 Advance Semiconductor Investigation - Power Transistor Ratings & Characteristics Which Are Important For Conversion Circuit Applications

5.5.1 Introduction

The purpose of this information is to familiarize the designer of power conversion circuits with transistor ratings and characteristics which are most pertinent and relevant to the selection and application of transistors as power circuit elements. The scope of this report will be limited to device considerations as applicable to circuits which are operating in the "switching mode" as opposed to linear operation. Because of the large number of conventions used in rating and specifying transistor parameters, it is felt that a summary investigation will serve to clarify definitions, symbols and characteristics as found in commercial data sheets. Hence, the primary purpose of this report will be to serve as a guide for interpreting and defining power transistor ratings and characteristics. The report is not intended to explain solid state theory as applied to transistor action.

At the present time, there are many conventions employed for stating transistor characteristics. One of the conventions is the "hybrid" or "h" parameter notation. The system is normally associated with low level signal and amplification circuits and is commonly referred to as the small signal characteristics. Another convention used to specify transistor parameters is the "large signal or D-C characteristics" system which as the name implies, relates transistor characteristics at high voltage and current levels. This system, which was pioneered by Ebers and Moll is uniquely applicable to germanium alloy junction transistors and is widely used to predict the behavior of transistors in power switching circuits. It is the D-C characteristics of transistors and their significance to power switching which will be discussed here.

The most common semiconductor materials that are used in the fabrication of power transistors are silicon and germanium. The limitations and capabilities of silicon and germanium devices are well known and documented. For the purpose of this report, it will be assumed that the primary criterion of maintaining the lowest possible voltage drop across the switching device during the high conduction interval is of utmost importance.

Based on this assumption, the germanium power transistor is presently the most favorable solid state switching device available.

The reason for placing a heavy weighting factor on the voltage drop across the transistor (normally referred to as the saturation voltage) during the conducting interval is related to the application of switching devices at low D-C supply voltage. At rated load, with a source voltage of 10 volts, a germanium transistor with a voltage drop in the order of 0.1 - 0.5 volts represents a significant difference in power loss as opposed to silicon devices with a 0.5 to 1.0 volt drop. The difference, of course, is more significant for source voltages less than 10 volts. Within this framework, transistor terminology, ratings, characteristics and symbols will be explained with emphasis on germanium devices.

5.5.2 General Description

Power transistors are manufactured in two basic configurations referred to as either NPN or PNP devices. The principal distinction from a practical point of view is one of current direction and voltage polarity in circuit application. Figures 5.5-3 and 5.5-4 illustrate the voltage polarity for NPN and PNP devices. Most high current, germanium junction devices are PNP structures; however, either silicon or germanium high current devices are available in NPN or PNP configurations. As shown in Figure 5.5-1 transistors are devices having three terminals which are identified as the base, emitter and collector. These terminals are analogous to the grid, cathode and anode of vacuum tube devices, respectively. It should also be noted that for any given NPN or PNP device, the only difference between the emitter and collector is the physical size of the junction and the impurity density or doping of the raw material. Complete physical symmetry in transistors is also possible and these devices are known as "bilateral" transistors.

In addition to the physical structural differences between transistors, added device flexibility and circuit utility is achieved by the placement of the device in circuit configurations referred to as: (1) common emitter (CE), (2) common base (CB), (3) common collector (CC). These configurations are illustrated in Figure 5.5-1. The configurations are characterized by differences in current gain, voltage gain, power gain, input impedance and output impedance, as well as phase relationships between input signals and output.

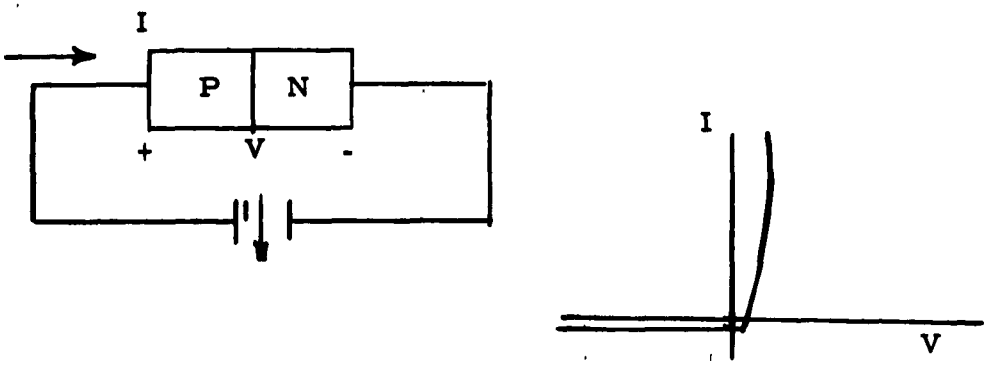
Of primary importance to this program, is the consideration and use of the transistor as an "ideal switch" for switching large currents. An "ideal switch" may be simply as having infinite impedance in the "off" position and zero resistance in the "on" position. This definition implies a lossless switch in both the conducting and non-conducting state. Further definitions may be stated for such factors as actuation time or transition time from a conducting to a non-conducting mode. The significance of this characteristic will become evident for dynamic switching of voltage and current.

The transistor does not, of course, meet the definitions of an ideal switch. By means of transistor ratings and characteristics, it is possible to assess a given transistor for use in switching circuits. Before examining the ratings and characteristics of transistors, a brief discussion of switching operation will be given.

The operation of a transistor as a switch can be divided into three regions; namely, the "on" or high conduction interval; the "off" or low conduction interval; and the linear region or the interval when the transistor operating point is traveling between the "on" and "off" state or conversely. The above defined regions are known as current saturation, collector current cutoff and linear regions respectively. Figure 5.5-2 illustrates these regions. It can be noted that point A is within the current saturation region and is characterized by a high current, low voltage state. Point B is shown within the current cutoff region and is characterized by a low current and high voltage standoff state. The linear region is shown as an area through which the operating point traverses in going to Point A or B. The path taken is a function of many variables and will not be discussed here other than noting that the speed at which the transition takes place and the path taken influence the losses in the power transistor and notably more so at higher frequencies.

The electrical concepts of how the operating regions are achieved can be illustrated by showing the polarities of instantaneous currents and voltages for the tree regions of operation. From Figure 5.5-3 it can be seen that the transistor is a three-layer device consisting of either PNP or NPN layers with corresponding terminals connected to each layer. Figure 5.5-3 is a pictorial representation of transistor currents and voltages for both PNP and NPN transistors connected in a common emitter configuration. The common emitter configuration has the greatest power gain and is most generally used in power conversion switching circuits.

In addition, Figure 5.5-3 represents the static conditions existing for the current saturation region. At this point in the discussion, it would be well to establish a reference for specifying polarities. A convenient reference is a simple two-layer diode inasmuch as the transistor can be thought of as two diodes utilizing a common base material. The static characteristics for a two layer diode are shown below.



Thus, when a forward voltage is applied to the P region of a giode, a resultant current flows. This condition is normally referred to as a "forward biased" one and constitutes + to - for a p-n junction. The same convention is used for transistors and in the case of a PNP device, the P-N junction associated with the emitter-base is often referred to as the emitter diode while the P-N junction associated with the collector-base is often referred to as the collector diode. Thus, for Figure 5.5-3d which shows transistor bias currents and voltage for the operating region of current saturation, both the emitter and collector junctions are forward biased. This definition applies as well to both the PNP and NPN configurations as shown in Figures 5.5-3c, d. Thus, for a PNP transistor to be in the saturated region, the base terminal must be less negative than the emitter terminal which results in a current flow out of the region as indicated in Figure 5.5-3d.

For the linear region of operation, (see Figure 5.5-4d), the emitter junction is forward biased while the collector junction is reverse biased. The corresponding polarities of voltages and currents are shown in Figure 5.5-4. It should be noted that although the directions of current flow are identical to the direction of current flow in the saturation region, the magnitudes are not identical. In switching applications, the linear region represents an area of very high instantaneous power dissipation.

It is therefore, extremely important to have very fast switching speeds so that the total average power dissipated is within limits.

The last region or the cutoff region is shown in Figure 5.5-5. During cutoff, the emitter and collector junctions are both reverse biased. In the "cutoff" region, the direction of currents are usually reversed and generally represent leakage currents with a magnitude determined by the transistor characteristics and circuit considerations. The "cutoff" region is representative of the open switch position and ideally should approach a condition of infinite impedance. The limitations of the transistor are reflected in the form of leakage currents at a given potential.

5.5.3 Ratings

A typical power transistor data sheet is divided into three areas of information. These areas are:

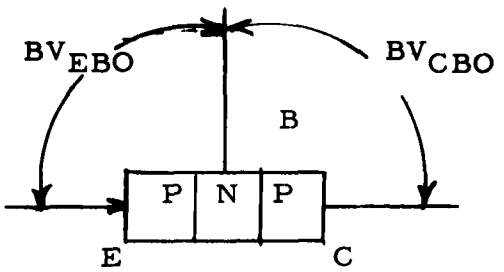
1. General information
2. Ratings
3. Characteristics

The general information as the name implies will give a brief description of the device identifying the material (germanium or silicon), the polarity (PNP or NPN); mechanical and physical data, power dissipation and a brief description of unique or special features. Although this is the first step into the entry of a data sheet, the degree of application data presented here is of minor importance in comparison to the stated ratings or characteristics. For this reason, the remainder of this discussion will be devoted to defining and explaining the ratings and characteristics.

A rating normally refers to the absolute maximum value of voltage or current to which a transistor may be subjected beyond which permanent degradation or damage may result. Ratings then define the extreme capabilities of a device and are normally given or stated by the manufacturer. Ratings are not considered design information, although they represent a logical step in the selection and application of a given power transistor. Typical data to be found under the category of ratings is shown in Table 5.5-1.

Items 1 through 5 of Table 5.5-1 deal with the voltage ratings of a given device. The prefix BV signifies "breakdown voltage" while the first two letters of the subscript indicate the junction or terminals between which the rating applies. The third letter in the subscript refers to the condition of the third terminal. The letter "O" signifies an open circuit condition; the letter R a given value of resistance between the third terminal and the terminal designated by the second subscript. Thus, BV_{CER} refers to the breakdown voltage between collector to emitter (first two letters of subscript), with a resistor of value R placed between the third terminal, base and emitter (identified in the second letter of subscript). Similarly, the subscript CES refers to the collector to emitter terminals with the base shorted to the emitter.

It should also be noted that the voltage ratings represent reverse bias conditions for the diode junctions. This is evident from the diagrams shown below for a PNP transistor.



In the case of BV_{EBO} and BV_{CBO}, the breakdown voltage is analogous to the peak reverse rating of a diode junction. In the case of BV_{CEO}, the breakdown voltage is a function of several parameters and in order to define as many variables as possible, the collector current or I_C should be specified.

Item 6 and item 7 represent absolute peak values of current which can be safely carried by the collector and base terminal respectively.

Item 8 relates to the maximum power dissipation capabilities of the device. From a standpoint of overall device capability, the thermal ratings of the device represent the basic fundamental limitations with respect to power handling capability. Power dissipation is influenced by the maximum allowable junction temperature. In the case of germanium devices, the limiting temperature is approximately 100°C while for silicon devices, it is approximately 200°C. A basic relationship is shown in Equation 5.5-1.

(5.5-1) $T_j = P_C \theta_{JA} + T_A$

where T_j = junction temperature, ^oC

P_C = avg. power dissipation, watts

θ_{JA} = total thermal resistance, $\frac{^oC}{W}$

T_A = ambient temperature, ^oC

Equation 5.5-1 can be rewritten as follows:

(5.5-2) $$P_C = \frac{T_j - T_A}{\theta_{JA}}$$

Equation 5.5-2 shows that the average power dissipation of a transistor is directly proportional to the temperature differential between the transistor junction and the ambient and inversely proportional to the thermal resistance of the transistor to the stated ambient. The total thermal resistance can be further defined and approximated as follows:

(5.5-3) $$\theta_{JA} = \theta_{JC} + \theta_{JS} + \theta_{SA}$$

where θ_{JA} = total thermal resistance (junction to ambient)

θ_{JC} = transistor thermal resistance (junction to case)

θ_{CS} = insulator thermal resistance (case to heat sink)

θ_{SA} = heat sink thermal resistance (heat to sink to ambient)

Rewriting Equation 5.5-2 and substituting into Equation 5.5-3, we now have:

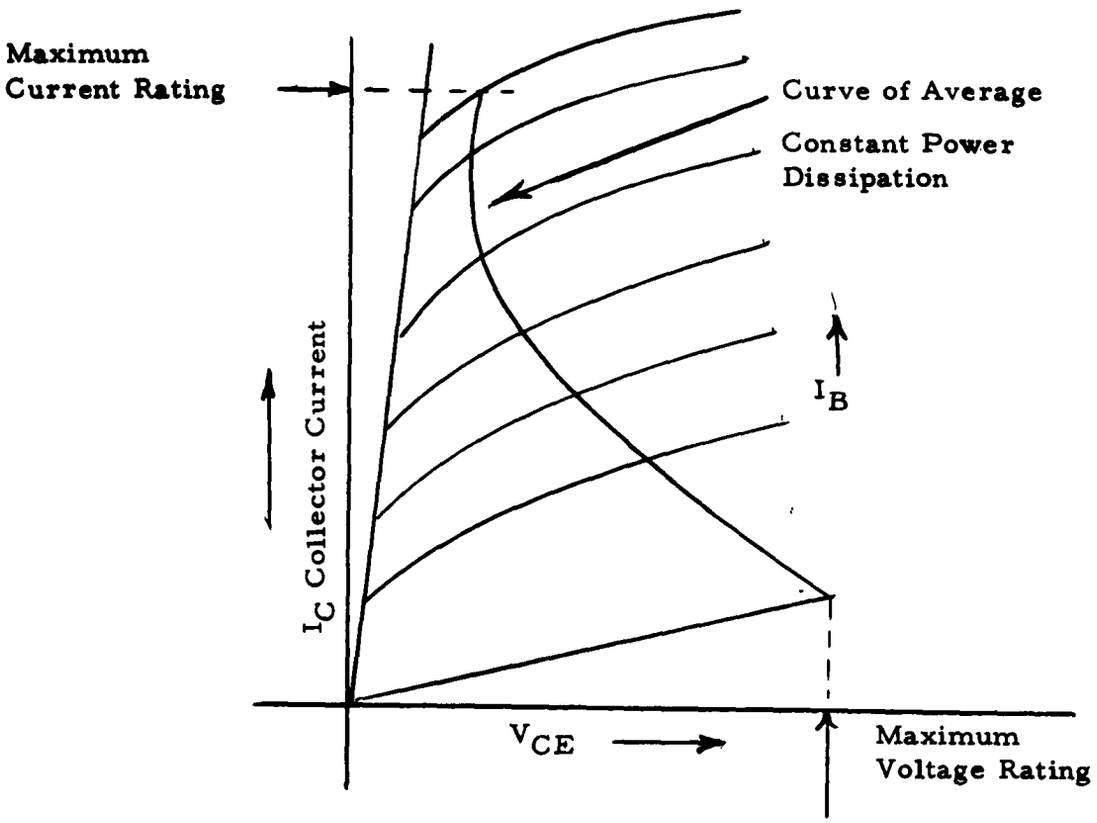
(5.5-4) $$P_C = \frac{T_j - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

From Equation 5.5-4 it can be seen that the power dissipation rating of a transistor is subject to considerable limitations. For instance, T_j is a fixed quantity depending on transistor material. T_A is a variable depending on application. Therefore, the manufacturer will specify a power dissipation rating at some ambient temperature. The thermal resistance from junction to case (θ_{JC}) is a quantity under total control of the manufacturer. The thermal resistance from case to heat sink is a quantity which can be considered under control of both the manufacturer and the designer. The manufacturer, of course, selects the physical configuration of the case, colors, materials, etc. However, the designer may or may not utilize such techniques as insulating the transistor from the heat sink, applying a lubricant between heat sink surface and the case of the transistor and the general mechanical considerations of mechanically mounting the transistor in a heat sink. The third component of the total thermal resistance is the thermal resistance from heat sink to ambient. Here the designer has complete control of the choice of heat sink.

From the above discussion, it can be seen that the power dissipation rating is an interdependent one involving many considerations. Considerable care must be exercized to operate the device within limitations which is subject to interpretation of manufacturer's data and application. It should also be noted that the above discussion is based on steady state considerations and does not apply to pulse power dissipation ratings which are dependent upon the thermal capacitance as well as the thermal resistance of the device.

One important point should be noted with regards to maximum transistor ratings. Absolute maximum current and absolute maximum voltage cannot be applied at the same time.

Thus, in order to rate a transistor in terms of power handling capability, it is not sufficient to take the product of the max. voltage and current rating since in steady state or linear operation the product of voltage and current must not exceed the power dissipation rating of a device. This power dissipation limitation is shown on the following characteristic transistor curves.



In switching applications, the transistor is normally operated from "cutoff" to "saturation" which limits the power dissipation to those losses which are incurred as a result of the fact that the transistor is not a perfect switch.

5.5.4 Characteristics

The portion of a specification sheet which is most useful to the design engineer are the electrical characteristics. The distinction between a rating and a characteristic is one where the non-linear properties of the device are presented in the form of specific electrical measurements. Here again, we have a wide variance between the nature and character of information presented by one manufacturer as contrasted to other manufacturers. Much of the transistor characteristics can be and usually are furnished in curves and represent typical values. Some of the characteristics are furnished in a table form and include minimum, typical and maximum values for specific test conditions.

Because of the temperature dependence of transistor characteristics, a mounting base or ambient temperature of 25°C is normally specified. The four common curves which illustrate "typical" characteristics are identified as follows:

a) Input characteristics

b) Output characteristics

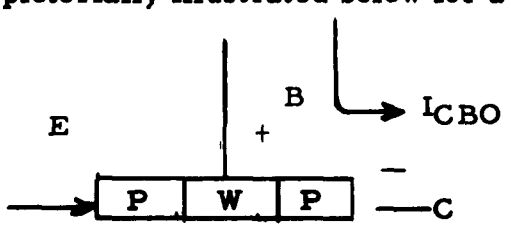
c) Current transfer characteristics

d) Transconductance characteristics

These curves represent the relationship between input and output currents and voltages for any one of the three transistor configurations (common emitter, common base, or common collector). The most widely presented curves are for the common emitter configuration because of the accuracy of representation and the ability to derive the characteristics for the other configurations from the common emitter configuration. Figure 5.5-6 illustrates typical characteristic curves for a Motorola power transistor Jan 2N 174. The curves are typical of those which may be furnished by other manufacturers.

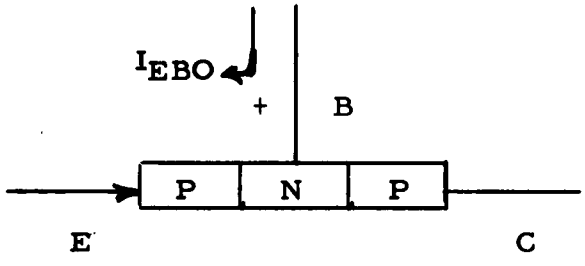
In addition to the characteristics which are presented in graphic form, a transistor specification sheet will also include a tabulation of data relating to currents, voltages and switching times which have been compiled at specific test points. Typical tabulated electrical characteristics which are found in a transistor specification sheet are shown in Table 5.5-2.

Items 1 and 2 refer to transistor leakage currents or currents below which "transistor" action ceases. I_{CBO} as described in Table 5.5-2 is pictorially illustrated below for a PNP device.

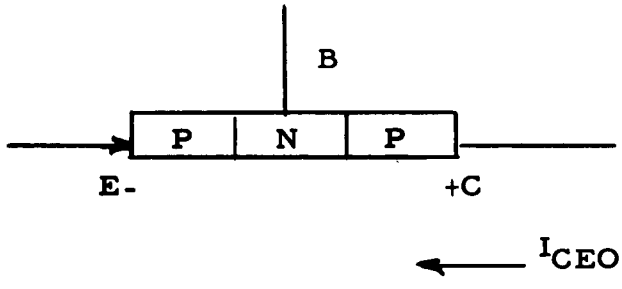


With the emitter terminal open circuited, I_{CBO} represents the leakage current of the collector junction normally measured at the BV_{CBO} rating of the device. I_{CB} represents the same current with a specified base to emitter bias.

Item 3 relates to the emitter diode leakage current as shown below for a PNP device.



With the collector terminal open-circuited, and the emitter junction reverse biased, I_{EBO} represents the emitter diode leakage currents. Item 4 (I_{CEO}) is a measure of the leakage current



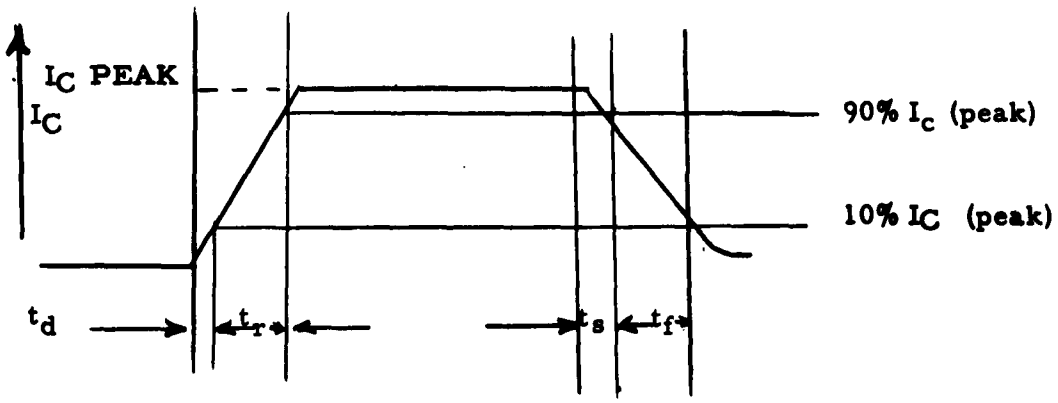
through the three layers of the device with a reverse bias applied across the collector to emitter terminals and the base open circuited. Item 5 (I_{CEX}) is the leakage current under the same conditions with the exception of a voltage applied to the base terminal.

Items 6 and 7 are normally given in curve form as shown in the input and transconductance characteristics of Figure 5.5-6. Item 8 refers to the saturation voltage $V_{CE(SAT)}$ or the minimum voltage required to maintain transistor action for a given collector and base current. This value is normally rated for one or two conditions of collector and base current. The "output characteristics" as are shown in Figure 5.5-6 are generally not expanded enough to yield accurate data below 1 volt V_{CE}.

Item 9 which is listed as h_{FE} represents the common emitter current gain or forward current transfer ratio. Here again, the value of h_{FE} is normally stated in terms of a dimensionless ratio for one or more values of I_C. It should be noted that h_{FE} is not constant for all values of I_C.

Item 10 represents the common emitter, small signal, forward current gain cutoff frequency. It is the frequency at which the current gain is .707 of the current gain value found at a given reference frequency. The .707 point represents a 3 db reduction in current gain where current gain is defined as $h_{FE} = \frac{I_C}{I_B}$. The reference frequency is normally 400 cps or 1000 cps. In most power switching applications, operation of the transistor beyond the cutoff frequency results in a severe derating of the capabilities of the power transistor.

Items 11 and 12 relate to the switching time of the transistors. Switching time is one of the most difficult parameters to measure since it is dependent upon other transistor variables as well as the circuit used by the manufacturer to measure turn "on" and turn "off" time. In power switching applications, the turn "on" and turn "off" time is the primary limitation in operating the transistor at a repetition rate above 2000 cps. The minimum information required to assess the turn "on" time is the collector current, I_C; and the base drive, I_B. It is also highly desirable to state the collector to emitter voltage V_{CE} prior to the conduction interval. (The reason for specifying the collector current and base drive is to determine the degree of transistor saturation which directly influences the storage time.) The most widely used convention for specifying the turn "on" time is based on stating the total turn "on" time which is composed of the delay time (t_d) and the rise time (t_r). The delay time is measured from the instant of base drive signal to a point where the collector current reaches 10% of the steady state value. The base drive current is considered to be a square wave pulse of constant amplitude. The rise time is then the interval of time when the collector current rises from 10% of its steady state value to 90% of its steady state value. The sum of the delay and rise time is then the total turn "on" time of the particular device.



t_d = delay time

t_s = storage time

t_r = rise time

t_f = fall time

The total turn'off'time is divided into two segments called the storage time and the fall time. As mentioned previously, storage time is a direct function of base drive current (amplitude and polarity) so that the conditions of the removal of base drive should be stated. However, in most cases, it is assumed that base drive current is merely reduced to zero in a step function. Thus, storage time is measured from the instant of removal of base drive to a point where the collector current drops off to 90% of the steady state value. (In many data sheets, a reverse bias is applied to the base which results in a shorter storage time). The fall time is then the interval of time when the collector current drops from 90% of its steady state value to 10% of the steady state value. The sum of the storage and fall time is then the total turn'off'time.

A listing of representative power transistors and their corresponding descriptions, ratings, and characteristics is given in Table 5.5-3.

TABLE 5.5-1

DC MEASUREMENTS - RATINGS

	SYMBOL	DESCRIPTION	COMMENTS
1.	BV_{CBO}	Collector diode breakdown voltage	Emitter open-circuited I_C should be specified.
2.	BV_{EBO}	Emitter diode breakdown voltage	Collector open-circuited I_E should be specified.
3.	BV_{CEO}	Collector emitter breakdown voltage	Base open-circuited I_C should be specified
4.	BV_{CER}	Collector emitter breakdown voltage	Resistor "R" between base and emitter.
5.	BV_{CES}	Collector emitter breakdown voltage	Base shorted to emitter
6.	I_C	Collector current	
7.	I_B	Base current	
8.	P_C	Power dissipation	Average continuous
9.	T_j	Junction temperature	Maximum and minimum

TABLE 5.5-2

POWER TRANSISTOR ELECTRICAL CHARACTERISTICS

SYMBOL		DESCRIPTION	COMMENTS
1.	I_{CBO}	Collector -base cutoff current or Collector diode current	Emitter open, collector junction reverse biased, state V_{CBO} as test condition
2.	I_{CB}	Collector diode current	Collector junction reverse biased, state V_{CB} and B_{EB} as test condition.
3.	I_{EBO}	Emitter -base cutoff current or Emitter diode current	Emitter junction is reverse biased and collector is open circuit, state V_{EBO} as test condition.
4.	I_{CEO}	Collector -emitter current	Collector junction reverse biased and base open circuited, state V_{CEO} as test condition.
5.	I_{CEX}	Collector -emitter current	Collector junction reverse biased, specified base to emitter voltage.
6.	V_{BE}	Base -to emitter voltage	Normally stated for a given I_B, I_C or V_{CE}.
7.	V_{EB}	"floating potential" emitter to base as a result of applying reverse bias to collector junction.	Normally stated at specified V_{CBO} with $I_E = 0$
8.	V_{CE} (SAT)	"Saturation voltage" from collector to emitter for a given I_C.	Minimum voltage necessary to sustain transistor action at a specified I_C and I_B.
9.	h_{FE}	Common emitter current gain or forward current transfer rates	$\frac{I_C}{I_B}$
10.	$f_{\alpha e}$	Common emitter current amplification cutoff frequency	Frequency at which h_{FE} drops to .707 of its original value where $h_{FE} \simeq \frac{I_C}{I_B}$

TABLE 5.5-2 (Cont'd)

POWER TRANSISTOR ELECTRICAL CHARACTERISTICS

SYMBOL	DESCRIPTION	COMMENTS
11. "on time"	t_d+t_r, delay and rise time associated with the rise of current in a transistor.	Normally measured from time t = 0 to a point where amplitude of the current pulse is .90 of maximum amplitude. Specify I_C and/or I_B, V_{CE}.
12. "off time"	t_s+t_f, storage and fall time associated with the fall of current in a transistor.	Normally measured from t = 0 to a point where the amplitude of current pulse is .10 of maximum amplitude. Specify I_C and/or I_B, V_{CE}.

WESTINGHOUSE

DESCRIPTION	WX118UA thru WX118UC	WX118XA thru WX118XB	2N1809 thru 2N1814	2N1816 thru 2N1819	2N1823 thru 2N1826
1. POLARITY	NPN	NPN	NPN	NPN	NPN
2. MATERIAL	Si	Si	Si	Si	Si
3. PROCESS	fused silicon	fused silicon	fused silicon	fused silicon	fused silicon
RATINGS					
1. P_C - Power Dissipation - watts	150 @ T_C = 45° C	150 @ T_C = 45° C	250 @ T_C = 60° C	250 @ T_C = 60° C	250 @ T_C = 60° C
2. I_C - Collector Current - amps	10	10	30	30	30
3. I_B - Base Current - amps	1.0	1.0	10	10	10
4. V_{CBO} - Collector - base, - volts emitter open circuit	50 - 150	50 - 150	50 - 300	50 - 200	50 - 200
5. V_{EBO} - Emitter - base, - volts collector open circuit	15	15	15	15	15
6. V_{CEO} - Collector - emitter - volts base open circuit	50 - 150	50 - 150	50 - 300	50 - 200	50 - 200
CHARACTERISTICS					
1. V_{CE} - Saturation voltage - volts	2.2 - 3.5 @ I_C = 10a, I_B =.15a	2.2 - 3.5 @ I_C = 10a, I_B =.15a	.4 - 1.5 @ I_C = 10a, I_B = 2a	.63 - 1.5 @ I_C = 15a, I_B = 3a	.74 - 1.5 @ I_C = 20a, I_B = 4a
2. I_{CEO} - Collector diode current - ma	-	-	-	-	-
3. I_{EBO} - Emitter diode current - ma	15 @ V_{BE} = -15 v, I_C = 0, T_C = 150°C	15 @ V_{BE} = -15 v, I_C = 0, T_C = 150°C	4 - 25 @ V_{EB} = 15v, I_C = 0, T_j = 175°C	4 - 25 @ V_{EB} = 15v I_C = 0, T_j = 175°C	4 - 25 @ V_{EB} = 15v I_C = 0, T_j = 175°C
4. I_{CEX} - Collector emitter leakage - ma	20 @ V_{CE} - max T_C=150°C, V_{BE}=-1.5v	20 @ V_{CE} - max T_C=150°C, V_{BE}=-1.5v	8 - 30 @ V_{CE} - max T_C=175°C, V_{BE}=-1.5v	8 - 30 @ V_{CE} - max T_C=175°C V_{BE}= 1.5v	8 - 30 @ V_{CE} - max T_C=175°C, V_{BE}= 1.5v
5. h_{FE} - Current gain	100 - 360 @ I_C = 10A, V_{CE} = 6 v	400 - 660 @ I_C = 10a, V_{CE} = 6v	7.5 @ I_C = 20a, V_{CE} = 4v	7.5 @ I_C = 25a, V_{CE} = 4v	7.0 @ I_C = 30a V_{CE} = 4v
6. ON TIME (t_d + t_r) - μ sec	10 @ I_C = 10a, V_{CE} = 12v	15 @ I_C = 10a, V_{CE} = 12v	12 @ I_C = 10a, V_{CE} = 12v	17 @ I_C = 15a, V_{CE} = 12v	20 @ I_C = 20a, V_{CE} = 12v
7. OFF TIME (t_s + t_f) - μ sec	30 @ I_C = 10a, V_{CE} = 12v	35 @ I_C = 10a, V_{CE} = 12v	14 @ V_{CE} = 12v, V_{BE} - 6v	13 @ V_{CE} = 12v, V_{BE} = -6v	15 @ V_{CE} = 12v, V_{BE} = - 6v

Table 5.5-3

DESCRIPTION	2N574A	2N575A	2N1157A	B1274	2N1031	2N1032	2N1651 thru 2N1653	2N2357 thru 2N2359
1. POLARITY	PNP	PNP	PNP	PNP	PNP	PNP	PNP	PNP
2. MATERIAL	Ge	Ge	Ge	Ge	Ge	Ge	Ge	Ge
3. PROCESS	alloy-junction	alloy-junction	alloy-junction	diffused alloy	-	-	diffused base	diffused alloy
RATINGS								
1. P_C - Power Dissipation - watts	100 @ T_C=25°C	100 @ T_C=25°C	100 @ T_C=25°C	60 @ T_C = 25°C	90 @ T_C = 25°C	90 @ T_C = 25°C	100 @ T_C = 25°C	170 @ T_C = 25°C
2. I_C - Collector Current - amps	25 (RMS)	25 (RMS)	25 (RMS)	10	15	15	25	50
3. I_B - Base Current - amps	2.5 (RMS)	2.5 (RMS)	2.5 (RMS)	-	-	-	-	-
4. V_{CBO} - Collector - base, - volts emitter open circuit	80	80	80	40 - 120	50 - 100	50 - 100	60 - 120	-
5. V_{EBO} - Emitter - base, - volts collector open circuit	-	-	-	-	-	-	1.5 @ I_{EBO} = 50ma, I_C = 0	2.5 @ I_B = 50ma, I_C = 0
6. V_{CEO} - Collector - emitter - volts base open circuit	-	-	-	40 - 120	20 - 70	20 - 70	30 - 80	30 - 80
CHARACTERISTICS								
1. V_{CE} - Saturation voltage - volts	.15 - .5	.15 - .5	.15 - .5	.5 - 1.0 @ I_C = 5a, I_B = .5a	.3 - 1.0 @ I_C =100a, I_B = 1a	.3 - 1.0 @ I_C = 10a, I_B = 1a	1.0 v @ I_C = 25a, I_B =2.5a	.9 @ I_C = 50a, I_B = 5a
2. I_{CBO} - Collector diode current - ma	-	-	-	20 @ BV_{CBO}	2 @ I_E = 0, V_{CB} = -60v	2 @ I_E = 0, V_{CB} = -60v	5 @ V_{CB} = -60v, I_E = 0	5 @ V_{CB} = -100v
3. I_{EBO} - Emitter diode current - ma	-	-	-	50 @ V_{EB} = .75, I_C = 0	1 - 2 @ V_{EB} = -10v, I_C = 0	1 - 2 @ V_{EB} = -10v, I_C = 0	-	-
4. I_{CEX} - Collector emitter leakage - ma	-	-	-	-	-	-	-	-
5. h_{FE} - Current gain	9 - 22 @ I_C = 10 a	19 - 42 @ I_C = 10 a	38 - 84 @ I_C = 10 a	50 - 120 @ I_C = 5.0a, V_{CE} = -2v	20 - 60 @ V_{CE} = -2v, I_C = 10a	50 - 100 @ V_{CE} = -2v, I_C = 10a	35 - 140 @ V_{CE} = -2v, I_C = 10a	15 @ I_C = 50a, I_B = 5a
6. ON TIME (t_d + t_r) - μ sec	-	-	-	-	15 I_C = 10a, I_B = 1a	15 I_C = 10a, I_B = 1a	7 I_C = 25a, I_B = 25a	-
7. OFF TIME (t_s + t_f) - μ sec	-	-	-	-	25 I_C = 10a, I_B = 1a	25 I_C = 10a, I_B = 1a	6.5 I_C = 25a, I_B = 2.5a	-

Table 5.5-3 (Cont)

	DELCO RADIO SEMICONDUCTOR PRODUCTS					MOTOROLA			
DESCRIPTION	2N1523	2N174	2N277	DTS-400	T-490	2N2079A thru 2N2082A	2N1162 thru 2N1167	2N2156 thru 2N2159	MP504 thru MP507
1. POLARITY	PNP	PNP	PNP	NPN	PNP	PNP	PNP	PNP	PNP
2. MATERIAL	Ge	Ge	Ge	Si	Ge	Ge	Ge	Ge	Ge
3. PROCESS	alloy-junction	alloy-junction	alloy-junction	tripple diffused	diffused base	alloy-junction	alloy-junction	alloy-junction	alloy-junction
RATINGS									
1. P_C - Power Dissipation - watts	30 @ T_C = 71° C	30 @ T_C = 71° C	15 @ T_C = 71° C	-	-	170 @ T_C = 25° C	90 @ T_C = 25° C	170 @ T_C = 25° C	170 @ T_C = 25° C
2. I_C - Collector Current - amps	50	15	50	5	10	15	25	30	60
3. I_B - Base Current - amps	8	4	4	1	-	-	-	-	-
4. V_{CBO} - Collector - base, - volts emitter open circuit	80	80	40	400	-	40 - 80	50 - 100	45 - 90	45 - 90
5. V_{EBO} - Emitter - base, - volts collector open circuit	30	60	20	5	-	20 - 40	25 - 50	25 - 45	25 - 45
6. V_{CEO} - Collector - emitter - volts base open circuit	60	55	25	400	280	25 - 65	-	30 - 75	30 - 75
CHARACTERISTICS									
1. V_{CE} - Saturation voltage - volts	.2 @ I_C = 50 a I_B = 5 a	.3 @ I_C = 12 a I_B = 5 a	.3 @ I_C = 12 a I_B = 2 a	.75 @ I_C = 5 a I_B = 1 a	.79 @ I_C = 5 a V_{BE} = .77	.7 - .9 @ I_C=12a I_B = 2 a	.3 to 1.0 @ I_C=25a I_B = 1.6 a	.2 to .3 @ I_C = 25a I_B = 2 a	.2 - .45 @ I_C = 30a, I_B = 5a
2. I_{CBO} - Collector diode current - ma	4 @ V_{CBO} = - 80 v	15 @ V_{CBO} = - 80 v	15 @ V_{CBO} = - 40 v	10 @ V_{CBO} = 400 v, T_C = 125° C	-	15 @ V_{CB} = V_{CB} max. I_E = 0, T_C = 71°C	10 - 20 @ V_{CB} = 15 T_C = 90°C	4 @ V_{CB} max I_E = 0, T_C = 71°C	4 - 15 @ V_{CB} max I_E = 0, T_C = 71°C
3. I_{EBO} - Emitter diode current - ma	8 @ V_{EBO} = - 30 v	1 @ V_{EBO} = - 60 v	1 @ V_{EBO} = - 20 v	-	3.9	4 @ V_{EB} = -40, I_C = 0	.5 @ V_{BE} = 12, I_C = 0	0.2 - 4 @ V_{EB} = -45, I_C = 0	0.2 - 4 @ V_{EB} = -45, I_C = 0
4. I_{CEX} - Collector emitter leakage - ma	-	-	-	I_{CES} = 10 @ V_{CES} = 400 v	5 @ 80 v V_{EB} = .5	-	-	-	-
5. h_{FE} - Current gain	37 @ I_C = 15 a V_{CE} = - 4 v	20 @ I_C = 12 a V_{CB} = - 2 v	25 @ I_C = 12 a V_{CB} = - 2	10 @ I_C = 5 V_{CE} = 5 v	-	8 @ I_C = 12 a V_{CB} = -2 v	15 - 65 @ V_{CE} = 1, I_C = 25a	15 - 38 @ I_C = 25a, V_{CB} = 2v	30 - 60, I_C = 15A 12 - 20, I_C = 50A
6. ON TIME (t_d + t_r) - μ sec	30	15	15	7	-	12	19	$f_{\alpha b}$ = 2.7 MC	$f_{\alpha b}$ = 3.6 MC
7. OFF TIME (t_s + t_f) - μ sec	30	15	15	9 (max)	-	13	21	-	-

Table 5.5-3 (Cont)

Common Base

Common Collector

Common Emitter

Figure 5.5-1

BASIC TRANSISTOR CIRCUIT CONFIGURATIONS

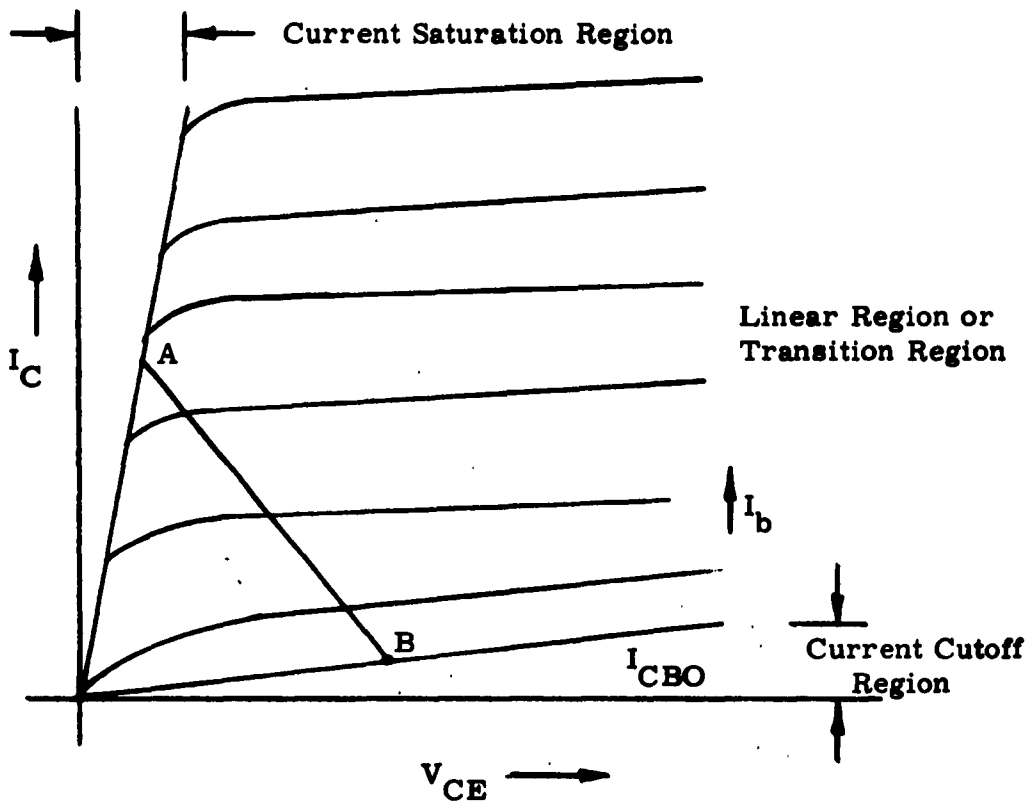
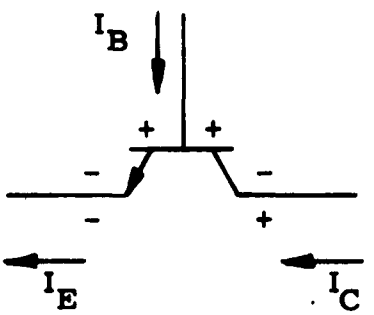


Figure 5. 5-2

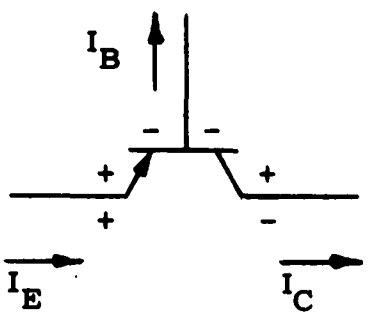
SIMPLIFIED COLLECTOR CHARACTERISTICS OF
COMMON - EMITTER TRANSISTOR SHOWING OPERATING REGIONS

NPN TRANSISTOR

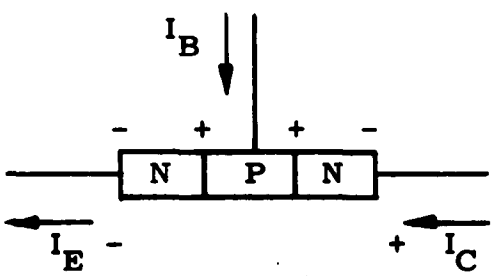


(a)

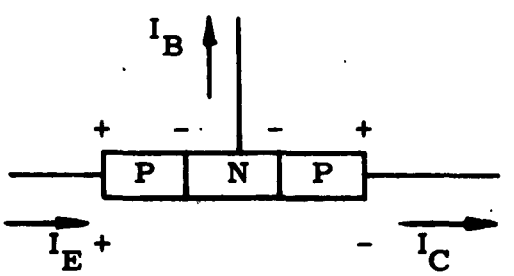
PNP TRANSISTOR



(b)



(c)



(d)

Figure 5.5-3

TRANSISTOR BIAS CURRENTS AND VOLTAGES
FOR SATURATION (ON) REGION OPERATION (COMMON EMITTER)

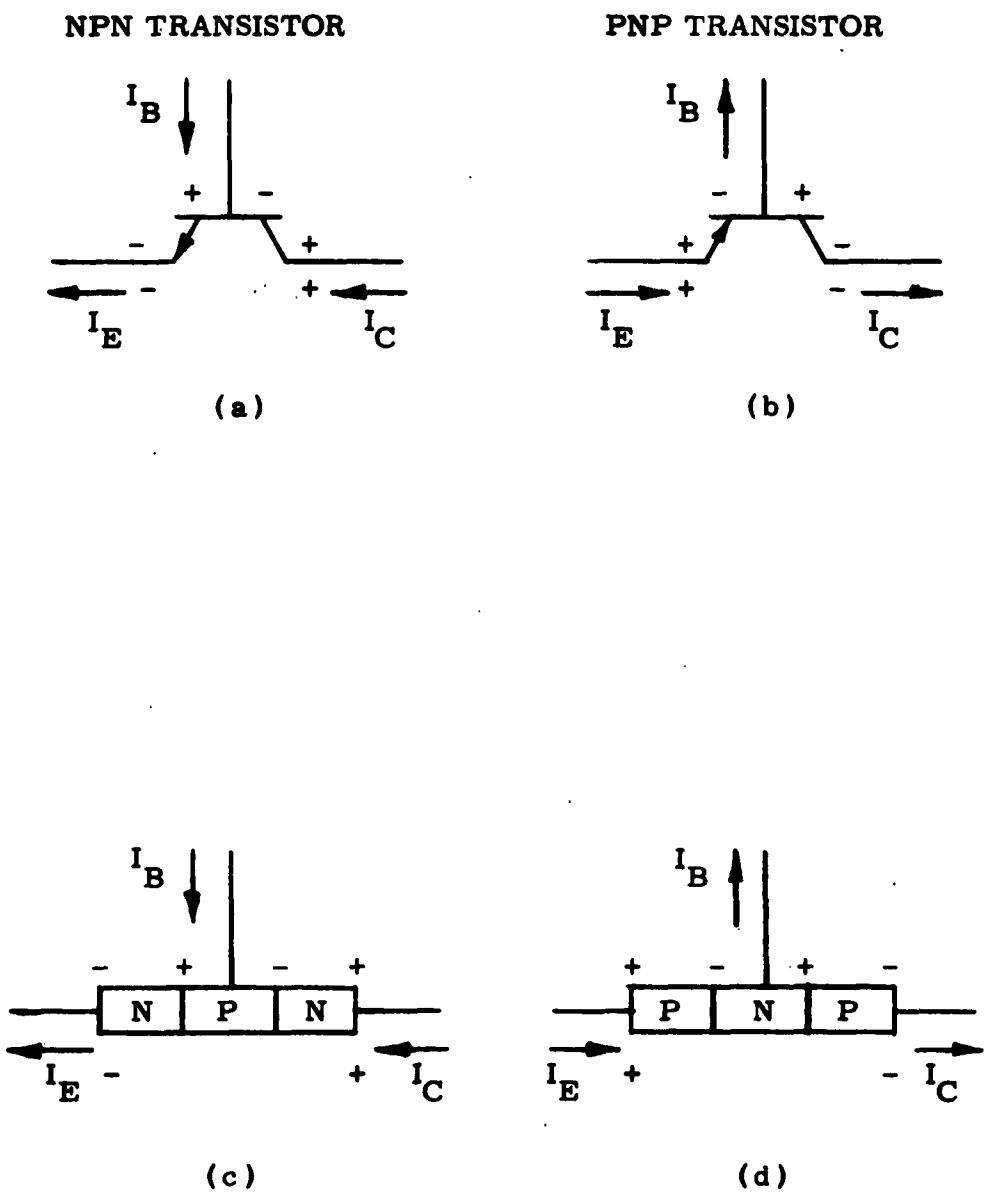


Figure 5.5-4

TRANSISTOR BIAS CURRENTS AND VOLTAGES FOR NORMAL LINEAR REGION OPERATION (COMMON EMITTER)

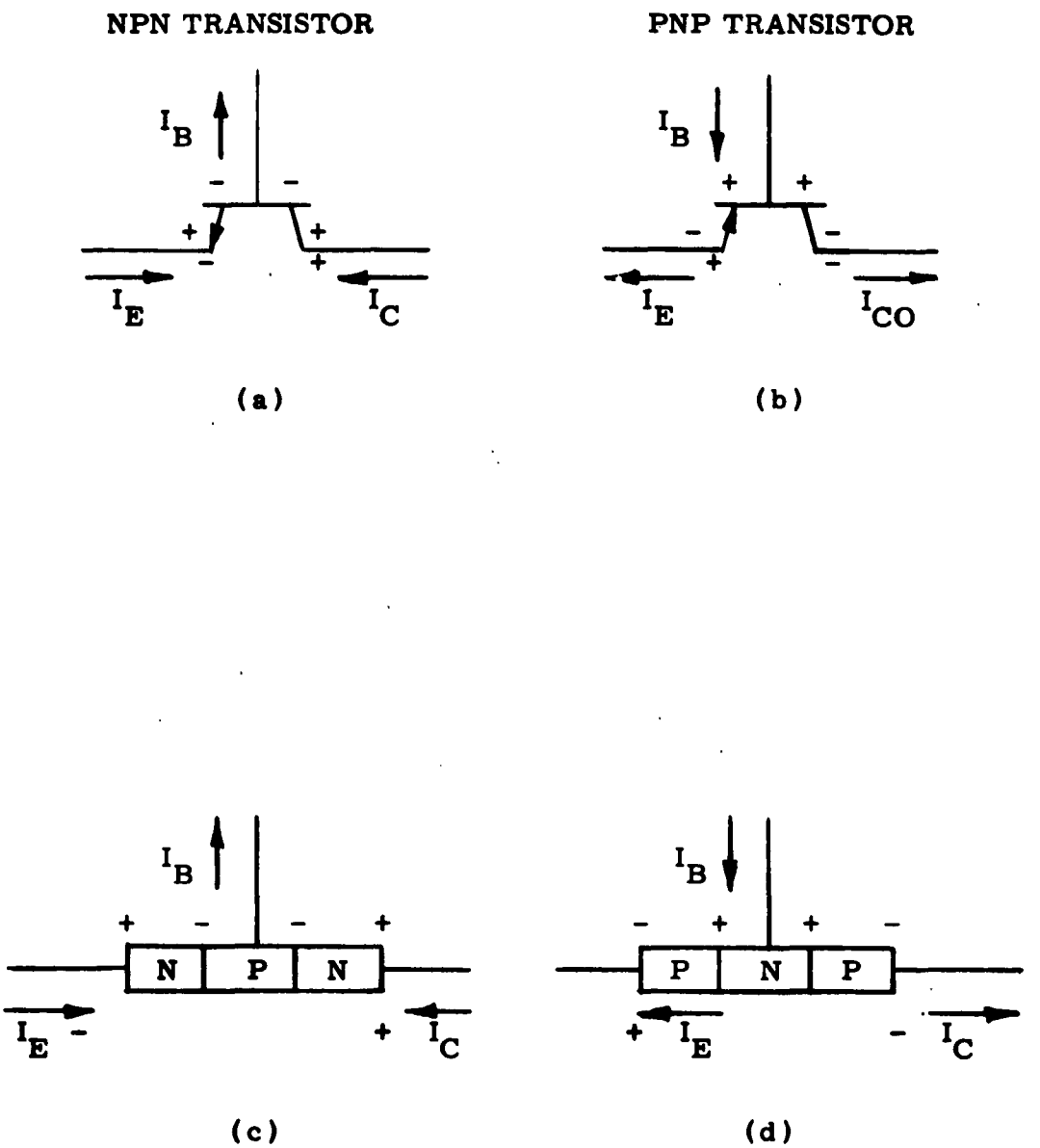


Figure 5.5-5

TRANSISTOR BIAS CURRENTS AND VOLTAGES FOR CUTOFF (OFF) REGION OPERATION (COMMON EMITTER)

TYPICAL CHARACTERISTICS,
COMMON EMITTER

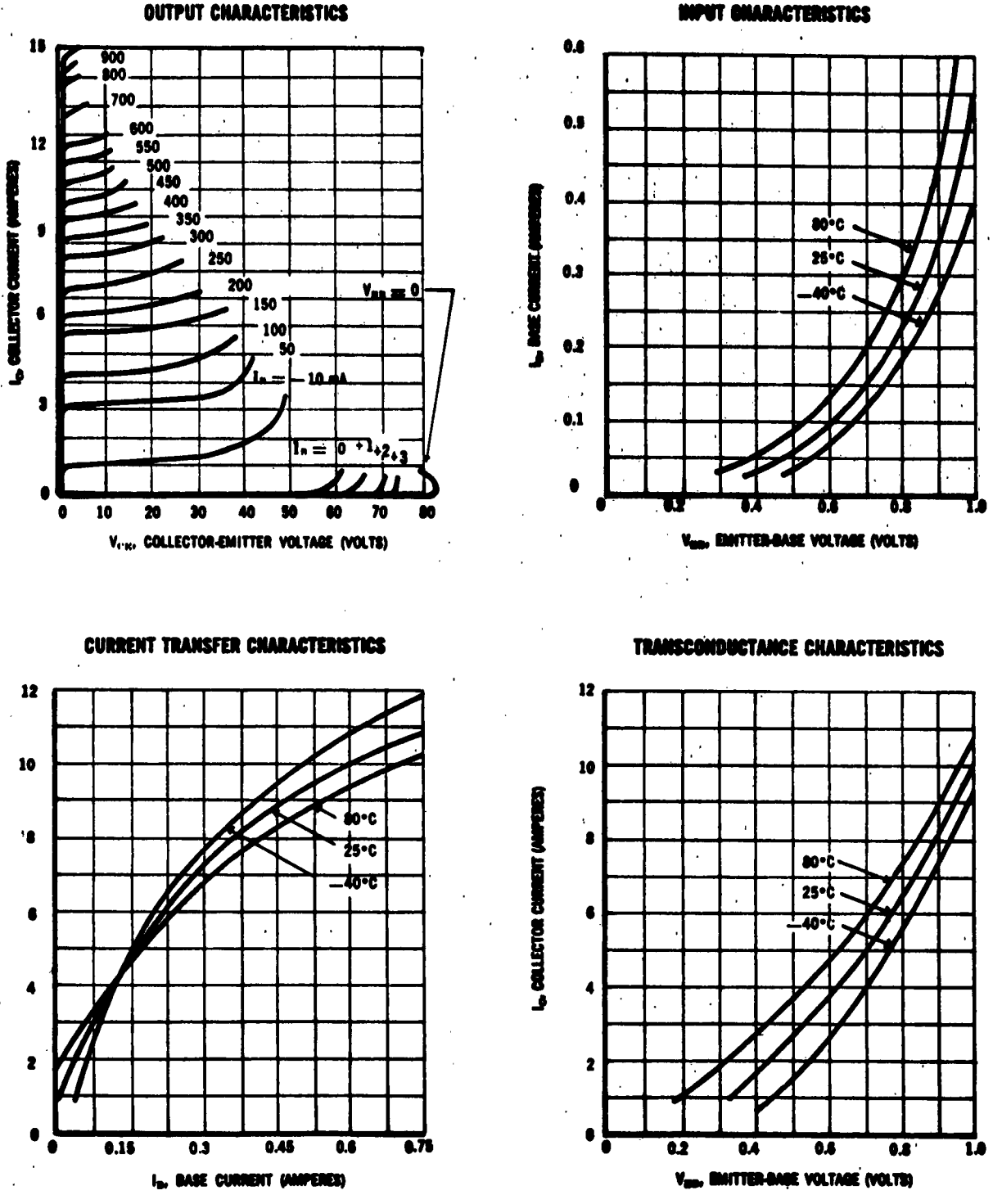


Figure 5.5-6

5.6 Advanced Circuit Concept Study

5.6.1 Nomenclature

a = Core leg width in inches (see Figure 5.6-1).

b = Core window width in inches (see Figure 5.6-1).

B = Maximum core flux density perturbation from average flux density level in webers per square inch.

C = Number of windings having rated volt-ampere rating.

e_c = Instantaneous induced voltage in coil under consideration in volts.

E_a = Average of absolute value of induced voltage in volts over one cycle for coil under consideration.

f = Frequency in cycles per second.

h = Core window height in inches (see Figure 5.6-1).

I = RMS current in amperes in coil under consideration.

J_c = RMS current density in amperes per square inch in coil wire.

K_c = Ratio of current carrying area or volume in total coil area or volume.

K_ℓ = Constant defining core loss in watts/in^3-$(cps)^n$($Webers/in^2$)^m.

n = Exponent defining the variation of core loss with frequency.

N = Number of turns on coil under consideration.

m = Exponent defining the variation of core loss with flux density.

P_i = Core loss in watts.

P_L = Total transformer loss in watts.

P_w = Total coil I^2R loss in watts.

t = Core leg depth in inches (see Figure 5.6-1).

T = $1/f$

= Period of a cycle in seconds.

V_i = Total volume of core in cubic inches.

V_w = Total volume of the windings in cubic inches.

W = Total weight of transformer in lbs.

α = Ratio of core loss per cubic inch to winding I^2R loss per cubic inch

$$= \frac{K_s K_f f^n B^m}{\sigma_w J_c^2 K_c}$$

γ_i = Factor defining the type of corners on core

$= \frac{\pi}{2}$ for round corners

= 2 for square core corners

γ_w = Factor defining type of corners on coil

$= \frac{\pi}{2}$ for round coil corners (probably true for all coils)

= 2 for square coil corners

ρ_i = Net density of the core in lbs/in^3.

ρ_w = Net density of the coils in lbs/in^3.

σ_w = Resistivity of current carrying material in ohm-inches.

ϕ = Instantaneous value of total flux at core in Webers.

ϕ_m = Maximum total core flux perturbation from the average value in Webers.

5.6.2 Introduction

Progress to date on the advanced circuit concept study is reported herein. This study is a theoretical investigation of various advanced DC to DC and DC to AC circuits in order to determine the merits of such circuits for use with unconventional power sources. Particular emphasis is placed on obtaining low weight, volume, and high efficiency. The objective is the attainment of lower weight, heigher efficiency circuits than presently available. It is presently intended that this be accomplished through optimum use of all components and through a combination of functions so as to use a minimum number of components. The Advanced Circuit Concept Study is divided into three primary phases. The first phase consists of a theoretical definition of the general component characteristics of weight, volume, and power losses. Such a definition is an essential prerequisite to the circuit evaluation to be performed in phases two and three. The components considered in this first phase include the magnetic components such as the inductors and transformers, the capacitors, the transistors and rectifiers plus their corresponding heat sinks. Phase two consists of the circuit synthesis and evaluation of various DC to DC circuits. This will be a repeating process involving the synthesis of a circuit, the calculation of its performance, and then utilization of the information gained to synthesize a new and better circuit. Phase three consists of the circuit synthesis and evaluation of various DC to AC circuits. The approach will be the same as that used for the DC to DC circuitry.

The effort to date has been devoted to Phase 1. Initial attention was given to the definition of the characteristics of the magnetic components such as the inductors and transformers. Results of this work are reported in the following paragraphs. The general analysis of the magnetic component is given in paragraph 6.3. Paragraph 6.4 shows the results, most of which are given in curve form and may be readily used for inductor or transformer design. A sample transformer design calculation is given in paragraph 6.5. This demonstrates how the results of this effort may be used.

5.6.3 Analysis

The following analysis is based upon a core type transformer or inductor as shown in Figure 5.6.1. The nomenclature used throughout the analysis is given in paragraph 5.6.1. The equations describing the characteristics of the magnetic component shown in Figure 5.6-1 may now be established.

The instantaneous induced voltage in any one coil is given by the following:

$$e_c = N \frac{d\phi}{dt}$$

Thus:

$$d\phi = \frac{e_c}{N} \, dt$$

Steady state-wise, the net excursion of magnetic flux (ϕ) over a complete cycle must be zero; thus from the above equation the average of the positive applied voltage must be equal to the average of the negative applied voltage. E_a is defined as the average of the absolute induced voltage for a given coil. Then if ϕ_m is defined as the maximum flux excursion from its average value, it is evident that the total flux change over a period is equal to $4\phi_m$. The relationship between ϕ_m and E_c then is:

$$4\phi_m = \frac{E_a T}{N}$$

The maximum flux excursion, ϕ_m, is related to a maximum flux density excursion, B_m, by the following expression:

$$\phi_m = at K_s B$$

Combining the above two equations and remembering that $T = 1/f$ the result is:

$$(5.6\text{-}1) \qquad at = \frac{E_a}{4fB K_s N}$$

For purposes of this analysis it will be assumed that all windings have the same current density and that each winding has the same volt ampere capability. If this is the case, then each winding will occupy the same amount of window space. Thus, if J_c is the current density and C is the number of coils on the transformer, then the current in a given coil is given by:

$$I = \frac{K_c J_c hb}{NC}$$

or:

$$(5.6\text{-}2) \qquad hb = \frac{INC}{K_c J_c}$$

In equation 5.6-2 J_c is the rms current density. This is in contrast to Equation 5.6-1 where E_a is an average and not an rms voltage.

Referring to Figure 5.6-1, the total iron core volume is

$$(5.6\text{-}3) \qquad V_i = 2ta\,(h + b + \gamma_i\, a)$$

In a similar manner, the total coil volume is:

$$(5.6\text{-}4) \qquad V_w = 2hb\left(t + a + \frac{\gamma_w b}{2}\right)$$

For purposes of this analysis it will be assumed that the core loss is proportional to the product of frequency to the n^{th} power in maximum flux density E to the m^{th} power. Thus, the power loss in the core is given by:

$$P_i = K_\ell\, K_s\, V_i\, f^n\, B^m$$

It will also be assumed that the coil loss or copper loss is proportional to the current density squared. Thus, the copper loss is given by:

$$P_w = \sigma_w\, J_c^{\,2}\, K_c\, V_w$$

The total loss is the sum of the iron loss and the copper loss and thus is given by:

$$(5.6\text{-}5) \qquad P_L = K_\ell\, K_s\, V_i\, f^n\, B^m + \sigma_w\, J_c^{\,2}\, K_c\, V_w$$

Neglecting structure, the total transformer weight is given by the following expression:

$$(5.6\text{-}6) \qquad W = \rho_i\, V_i + \rho_w\, V_w$$

Equations 5.6-1 through 5.6-6 describe the weight, power loss and dimensions of a general transformer of the core type. Equations 5.6-1 through 5.6-4 may now be combined with Equation 5.6-5 so as to eliminate t, h, V_i and V_w thus yielding:

$$(5.6\text{-}7)\quad P_L = \frac{K_\ell f^n B^m E_a}{2fB}\left[\frac{CI}{K_c J_c b} + \frac{b\left(1 + \Psi_i \frac{a}{b}\right)}{N}\right] + 2\sigma_w J_c^2 IC\left[\frac{E_a}{4K_s fBb\left(\frac{a}{b}\right)} + Nb\left(\frac{a}{b} + \frac{\Psi_w}{2}\right)\right]$$

In a similar manner, Equations 5.6-1 through 5.6-4 may be combined with Equation 5.6-6 so as to eliminate t, h, Ψ_i, and V_w and yielding:

$$(5.6\text{-}8)\quad W = \frac{CE_a I \rho_w}{2K_s K_c fB J_c a}\left[1 + \frac{\rho_i}{\rho_w}\frac{a}{b}\right] + \frac{2INC\rho_w b\left(\frac{a}{b} + \frac{\Psi_w}{2}\right)}{K_c J_c} + \frac{E_a \rho_i b\left(1 + \Psi_i \frac{a}{b}\right)}{2K_s fBN}$$

Equations 5.6-7 and 5.6-8 describe the power loss and and weight of a transformer in terms of variables b, $\frac{a}{b}$, N, B and current density J_c. In this case the optimum combination of these variables which will yield a minimum weight transformer for a given power loss is desired. In this analysis, J_c and B will initially be considered fixed quantities and the optimum combination of b, N and $\frac{a}{b}$ will be determined for these conditions. A later optimization will consider J_c and B as variables. Before proceeding, it is desirable to simplify equations 5.6-7 and 5.6-8 by choosing an appropriate non-dimensional grouping of quantities. Thus, if we let:

$$\bar{b} = \frac{b(K_s K_c fB J_c)^{1/4}}{(E_a IC)^{1/4}}$$

$$\bar{N} = \frac{N(IfBCK_s)^{1/2}}{(E_a K_c J_c)^{1/2}}$$

$$\overline{P}_L = \frac{P_L (K_s K_c fB J_c)^{3/4}}{(E_a IC)^{3/4} (\sigma_w J_c^2 K_c)}$$

$$\overline{W} = \frac{W(K_s K_c fB J_c)^{3/4}}{\rho_i (E_a IC)^{3/4}}$$

$$\alpha = \frac{K_s K_\ell f^n B^m}{\sigma_w J_c^2 K_c}$$

Then Equations 5.6-7 and 5.6-8 become:

$$(5.6\text{-}9) \quad \overline{P_L} = \frac{\alpha}{2}\left[\frac{1}{\overline{b}} + \frac{\overline{b}}{\overline{N}}\left(1 + \gamma_i \frac{a}{b}\right)\right] + 2\left[\frac{1}{4\overline{b}\left(\frac{a}{b}\right)} + \overline{b}\overline{N}\left(\frac{a}{b} + \frac{\gamma_w}{2}\right)\right.$$

$$(5.6\text{-}10) \quad \overline{W} = \frac{\left(1 + \frac{\rho_i}{\rho_w}\frac{a}{b}\right)}{2\overline{b}\left(\frac{\rho_i}{\rho_w}\right)\left(\frac{a}{b}\right)} + \frac{2\overline{b}\overline{N}\left(\frac{a}{b} + \frac{\gamma_w}{2}\right)}{\left(\frac{\rho_i}{\rho_w}\right)} + \frac{\overline{b}\left(1 + \gamma_i \frac{a}{b}\right)}{2\overline{N}}$$

The relationship 5.6-11 and 5.6-12 describe Equations 5.6-9 and 5.6-10 in a general form.

$$(5.6\text{-}11) \quad \overline{P_L} = f\left(\overline{b}, \overline{N}, \frac{a}{b}\right)$$

$$(5.6\text{-}12) \quad \overline{W} = f\left(\overline{b}, \overline{N}, \frac{a}{b}\right)$$

Now the values of $\overline{b}$, $\overline{N}$, and $\frac{a}{b}$ are desired which will yi minimum weight for a given power loss. Minimum weight can be determined by letting:

$$(5.6\text{-}13) \quad d\overline{W} = \frac{\partial \overline{W}}{\partial \overline{b}} d\overline{b} + \frac{\partial \overline{W}}{\partial \overline{N}} d\overline{N} + \frac{\partial \overline{W}}{\partial\left(\frac{a}{b}\right)} d\left(\frac{a}{b}\right) = 0$$

Subject to the constraint that,

$$(5.6\text{-}14)\quad d\bar{P}_L = \frac{\partial \bar{P}_L}{\partial \bar{b}}\, d\bar{b} + \frac{\partial \bar{P}_L}{\partial \bar{N}}\, dN + \frac{\partial \bar{P}_L}{\partial\left(\frac{a}{b}\right)} d\left(\frac{a}{b}\right) = 0$$

Solving Equation 5.6-14 for $d\bar{b}$ and substituting this in Equation 5.6-13 to eliminate $d\bar{b}$ yields:

$$(5.6\text{-}15)\quad \left[\frac{\partial \bar{W}}{\partial \bar{N}} - \frac{\left(\frac{\partial \bar{W}}{\partial \bar{b}}\right)\left(\frac{\partial \bar{P}_L}{\partial \bar{N}}\right)}{\left(\frac{\partial \bar{P}_L}{\partial \bar{b}}\right)}\right] d\bar{N} + \left[\frac{\partial \bar{W}}{\partial\left(\frac{a}{b}\right)} - \frac{\left(\frac{\partial \bar{W}}{\partial \bar{b}}\right)\left(\frac{\partial \bar{P}_L}{\partial\left(\frac{a}{b}\right)}\right)}{\left(\frac{\partial \bar{P}_L}{\partial \bar{b}}\right)}\right] d\left(\frac{a}{b}\right)$$

$$= 0$$

Since $d\bar{N}$ and $d\left(\frac{a}{b}\right)$ can take on values independently of each other, it is evident that Equation 5.6-15 can only be true if the coefficients of $d\bar{N}$ and $d\left(\frac{a}{b}\right)$ are zero. Thus:

$$(5.6\text{-}16)\quad \left[\left(\frac{\partial \bar{W}}{\partial \bar{N}}\right)\left(\frac{\partial \bar{P}_L}{\partial \bar{b}}\right) - \left(\frac{\partial \bar{W}}{\partial \bar{b}}\right)\left(\frac{\partial \bar{P}_L}{\partial \bar{N}}\right)\right] = 0$$

$$(5.6\text{-}17)\quad \left[\left(\frac{\partial \bar{W}}{\partial\left(\frac{a}{b}\right)}\right)\left(\frac{\partial \bar{P}_L}{\partial \bar{b}}\right) - \left(\frac{\partial \bar{W}}{\partial \bar{b}}\right)\left(\frac{\partial \bar{P}_L}{\partial\left(\frac{a}{b}\right)}\right)\right] = 0$$

Substituting Equation 5.6-9 and 5.6-10 into Equation 5.6-16 and performing the required algebraic manipulation yields:

$$(5.6\text{-}18)\quad \bar{b}^2 = \frac{\left[1 + \gamma_i \frac{a}{b} + 4\bar{N}^2\left(\frac{a}{b}\right)\left(\frac{a}{b} + \frac{\gamma_w}{2}\right)\right]}{8\bar{N}\left(\frac{a}{b}\right)\left(\frac{a}{b} + \frac{\gamma_w}{2}\right)\left(1 + \gamma_i \frac{a}{b}\right)}$$

In a similar manner substituting Equation 5.6-9 and 5.6-10 into Equation 5.6-17 yields:

For any given $\frac{a}{b}$, Equation 5.6-22 gives the optimum b, Equation 5.6-21 gives the optimum N, and Equation 5.6-10 gives either the minimum or maximum weight, W, for the power loss, P_L, given by Equation 5.6-9. Thus, it is evident that the numerical results can be readily obtained from these equations. The procedure is to select a ρ_i/ρ_w, α, and $\frac{a}{b}$. b, n, W and P_L may then be calculated. This has been done and the results are shown in Figures 5.6-4 through Figure 5.6-7. Figure 5.6-4 shows the minimum weight versus power loss for various values of α and ρ_i/ρ_w. Only the minimum weight portion of the curve is shown. Figure 5.6-6 and Figure 5.6-7 show the corresponding N and b as a function of $\frac{a}{b}$ and α. Figures 5.6-8 through 5.6-11 are curves showing the limiting case of the general data given in Figure 5.6-4. Figure 5.6-8 shows the minimum possible transformer weight, while Figure 5.6-9 shows the corresponding power loss for this minimum weight transformer. Figure 5.6-11 shows the minimum power loss transformer while Figure 5.6-10 shows the corresponding weight for this minimum power loss transformer.

Figure 5.6-4 is adequate for the conditions where a fixed current density (J_c) and a fixed flux density (B) have been chosen. However, the optimum J_c and B for a minimum weight transformer are not evident since both J_c and B appear in the ordinant, the absissa and α. However, J_c may be easily eliminated from the ordinant by multiplying the ordinant values by α to the 3.75 power. In a similar manner, J_c can be eliminated from the absissa by multiplying absissa values by α to the negative 6.25 power. This was done and the results are shown in Figure 5.6-2. The corresponding values of $\frac{a}{b}$ are given in 5.6-3. The information given by Figures 5.6-2 and 5.6-3 is most useful in a general transformer design. This is illustrated in the calculation of paragraph 5.6-5.

5.6.4 Summary of Results

The following equations summarize the results of the analysis. For a selected ratio of $\frac{a}{b}$ the optimum value of dimension b of Figure 5.6-1 is:

$$(5.6\text{-}22a) \quad b^2 = \frac{(E_a\, IC)^{1/2}\,(1+\tau)}{4(K_s\, K_c\, fB\, J_c)^{1/2}\left(\frac{a}{b}\right)^{1/2}\left(\frac{a}{b}+\frac{\gamma_w}{2}\right)^{1/2}\left(1+\gamma_i\frac{a}{b}\right)^{1/2}\tau^{1/2}}$$

where: $\tau = 1.0$

or: $$\tau = \frac{\left(\frac{\gamma_i \gamma_w}{2} + 1\right) + \gamma_w\left(\frac{b}{a}\right)}{\left[\frac{\gamma_i \gamma_w}{2} + 1 + 2\gamma_i \frac{a}{b}\right]}$$

The optimum number of turns is:

$$(5.6\text{-}21a) \quad N^2 = \frac{(E_a K_c J_c)\left(1 + \gamma_i \frac{a}{b}\right)\tau}{4(ICFB\, K_s)\left(\frac{a}{b}\right)\left(\frac{a}{b} + \frac{\gamma_w}{2}\right)}$$

The optimum value of dimension "a" of Figure 5.6-1 is:

$$(5.6\text{-}1a) \quad t = \frac{E_a}{4fB\, K_s\, Na}$$

The optimum value of dimension "h" of Figure 5.6-1 is:

$$(5.6\text{-}2a) \quad h = \frac{INC}{K_c J_c b}$$

The power loss for a transformer having the preceding dimension is:

$$(5.6\text{-}7a) \quad P_L = \frac{K_2 f^n B^m E_a}{2fB}\left[\frac{CI}{K_c J_c b} + \frac{\left(b\ 1 + \gamma_i \frac{a}{b}\right)}{N}\right] + 2\sigma_w J_c^2 IC\left[\frac{E_a}{4K_s fBb\left(\frac{a}{b}\right)} + Nb\ \frac{a}{b} + \frac{\gamma_w}{2}\right]$$

The corresponding weight for a transformer of these dimensions is:

$$(5.6\text{-}8a) \qquad W = \frac{CE_a I \rho_w}{2K_s K_c fB J_c a}\left[1 + \frac{\rho_i}{\rho_w}\frac{a}{b}\right] + \frac{2INC\,\rho_w\, b\left(\frac{a}{b} + \frac{\gamma_w}{2}\right)}{K_c J_c} + \frac{E_a \rho_i b\left(1 + \gamma_i \frac{a}{b}\right)}{2K_s fBN}$$

The results are presented in a much more useful form in the curves of 5.6-2 through 5.6-11. A given value of weight, power loss, and flux density specify a design point on the curves of Figure 5.6-2. This design point sets the value of α from which the current density J_c can be calculated. The curves of Figure 5.6-3 may then be used to determine $\frac{a}{b}$. The number of turns N and the dimension b may be determined using the curves of Figures 5.6-6 and 5.6-7. The remaining transformer dimensions can then be easily calculated using the equations indicated previously. If both the current density J_c and the flux density B are selected prior to the transformer design, the curves given in Figures 5.6-4 and 5.6-5 may be used in lieu of the curves of Figures 5.6-2 and 5.6-3.

It will be noted that the curves given in Figures 5.6-3, 5.6-5, 5.6-6 and 5.6-7 are shown in both dotted and solid lines. This results from the fact that either of two possible number of turns may be used and still achieve minimum weight for a given power loss. Use of the solid line curves will yield a transformer with a minimum number of turns. Use of the dotted line curves will yield a transformer with greater than minimum number of turns. Usually the transformer with minimum turns is the more desired one.

5.6.5 Sample Transformer Design Calculation

The use of the design information presented herein is best illustrated by means of a simple transformer design calculation. It will be assumed that a two winding 400 cycle transformer is desired which has a minimum weight for a given power loss. The transformer is to have a 100 volt-ampere rating and the rated voltage of one of the windings is 115 volts. Selectron iron core material with 4 mil laminations will be used. The other pertinent constants are:

a) Core lamination stacking factor (K_s) = 0.90

b) Core winding factor (K_c) = .40

c) Core losses proportional to $K_\ell f^n B^m$

$n = 1.3$

$m = 1.7$

$K_\ell = 153$

d) Number of windings (c) = 2.0

e) Copper resistivity (σ_w) = $.735 \times 10^{-6}$ ohm-inch

f) Frequency (f) = 400 cps

g) Volt-ampere rating = 100

h) E_{rms} = 115 volts

Thus

$$E_a = \frac{2\sqrt{2}}{\pi} E_{rms}$$

$$= 103.5 \text{ volts}$$

i) $I = \frac{100}{115} = .87$ amps rms

j) Core density (ρ_i) = $.272 K_s$

$= .245$ lbs/in^3

k) Coil density (ρ_w) = $.32 K_c$

$= .128$ lbs/in^3

l) $\frac{\rho_i}{\rho_w} = 1.915$

m) Core saturation flux density = 15000 lines/cm^2

$= 9.69 \times 10^{-4}$ webers/in^2

Thus:

$$\frac{P_L(K_s K_c fB)^{3/4}}{(E_a IC)^{3/4}(\sigma_w K_c)^{3/8}(K_s K_\ell f^n B^m)^{5/8}}$$

$$= \frac{P_L(.90 \times .40 \times 400B)^{3/4}}{(103.5 \times .87 \times 2.0)^{3/4}(.735 \times 10^{-6} \times .40)^{3/8}(.90 \times 153 \times 400^{1.3} \times B^{1.7})^{5/8}}$$

$$= .733\, P_L\left(\frac{B}{9.69 \times 10^{-4}}\right)^{.312}$$

and:

$$\frac{W(K_s K_c fB)^{3/4}(K_s K_\ell f^n B^m)^{3/8}}{\rho_i(E_a IC)^{3/4}(\sigma_w K_c)^{3/8}}$$

$$= \frac{W(.90 \times .40 \times 400B)^{3/4}(.90 \times 153 \times 400^{1.3} \times B^{1.7})^{3/8}}{.245(103.5 \times .87 \times 2.0)^{3/4}(.735 \times 10^{-6} \times .40)^{3/8}}$$

$$= 7.53\, W\left(\frac{B}{9.69 \times 10^{-4}}\right)^{1.388}$$

where:

$$B = \text{webers/in}^2$$

Data points at a ρ_i/ρ_w of 1.915 may be obtained from Figure 5.6-2. These in turn may be translated into actual weight and power loss data. Curves showing actual weight and power loss for this transformer are given for various maximum flux densities in Figure 5.6-12. The design point indicated on these curves was chosen. At this design point:

$$P_L = 5.33 \text{ watts}$$

$$W = .47 \text{ lbs.}$$

Thus at this point:

$$\frac{P_L (K_s K_c f B)^{3/4}}{(E_a IC)^{3/4} (\sigma_w K_c)^{3/8} (K_s K_\ell f^n B^m)^{3/8}} = .733 P_L$$

$$= .733 \times 5.$$

$$= 3.91$$

From Figure 5.6-2, at this point, for a $\rho_i/\rho_w = 1.915$:

$$\alpha = 1.4$$

and from Figure 5.6-3:

$$\frac{a}{b} = .7$$

for the case of minimum number of turns.

From Figure 5.6-6:

$$\frac{N(K_s CIfB)^{1/2}}{(K_c J_c E_a)^{1/2}} = 0.71$$

and from Figure 5.6-7

$$\frac{b(K_s K_c fB J_c)^{1/4}}{(E_a IC)^{1/4}} = 0.582$$

However:

$$\alpha = \frac{K_\ell K_s f^n B^m}{\sigma_w J_c^2 K_c}$$

Thus:

$$J_c = \sqrt{\frac{K_s K_\ell f^n B^m}{\sigma_w K_c}}$$

$$= \sqrt{\frac{.90 \times 153 \times 400^{1.3} \times (0.69 \times 10^{-4})^{1.7}}{.735 \times 10^{-6} \times .40 \times 1.4}}$$

$$\underline{\underline{J_c}} = \underline{\underline{2475 \text{ amps/in}^2}}$$

Thus:

$$N = \frac{.71(K_c J_c E_a)^{1/2}}{(K_s CIfB)^{1/2}}$$

$$= \frac{.71(.40 \times 2475 \times 103.5)^{1/2}}{(.90 \times 2 \times .87 \times 400 \times 9.69 \times 10^{-4})^{1/2}}$$

$$\underline{\underline{N}} = \underline{\underline{292 \text{ turns}}}$$

Also:

$$b = \frac{.582(E_a IC)^{1/4}}{(K_s K_c fB J_c)^{1/4}}$$

$$= \frac{.582(103.5 \times .87 \times 2)^{1/4}}{(.90 \times .40 \times 400 \times 9.69 \times 10^{-4} \times 2475)^{1/4}}$$

$$\underline{b} = \underline{.495 \text{ inches}}$$

Of course:

$$a = b\left(\frac{a}{b}\right)$$

$$= 0.495 \times 0.70$$

$$\underline{a} = \underline{.347 \text{ inches}}$$

And:

$$t = \frac{E_a}{4K_s fB\, Na}$$

$$= \frac{103.5}{4 \times .90 \times 400 \times 9.69 \times 10^{-4} \times 292 \times .347}$$

$$\underline{t} = \underline{.733 \text{ inches}}$$

Also:

$$h = \frac{INC}{K_c J_c b}$$

$$= \frac{.87 \times 292 \times 2}{.40 \times 2475 \times .495}$$

$$\underline{h} = \underline{1.037 \text{ inches}}$$

The preceding quantities determine the pertinent parameters of a minimum weight, two winding transformers for a chosen power loss. The number of turns required on the second winding can be determined by selecting the proper turns ratio to give the required voltage ratio. The wire size in each winding should be chosen so as to achieve the indicated current density of 2475 amps per square inch.

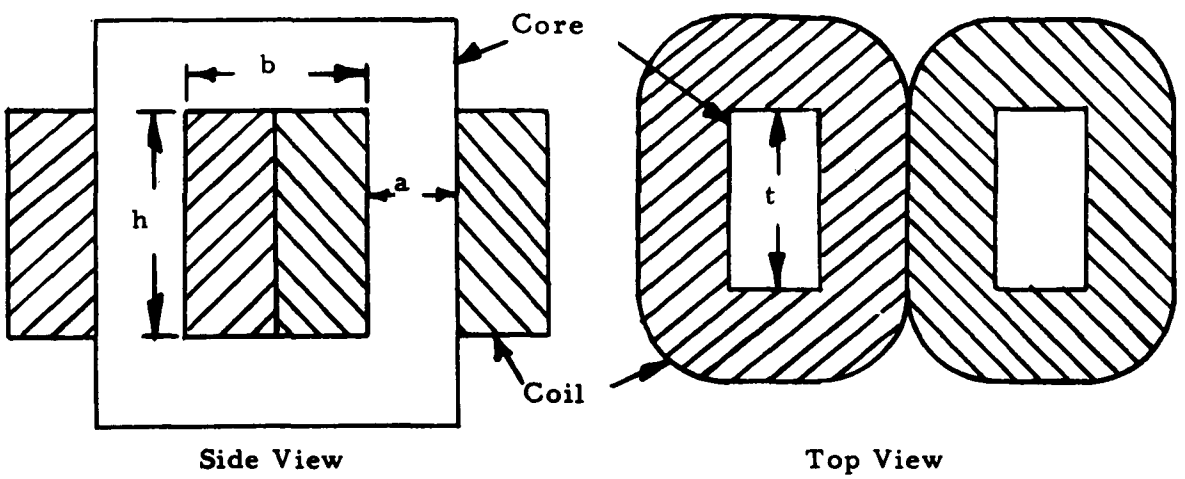


Figure 5.6-1: Core Type Transformer Cross Sectional Views

Figure 5.6-2: Minimum Weight as a Function of Power Loss, Magnetic Flux, Density Change, Core Density, and Coil Density

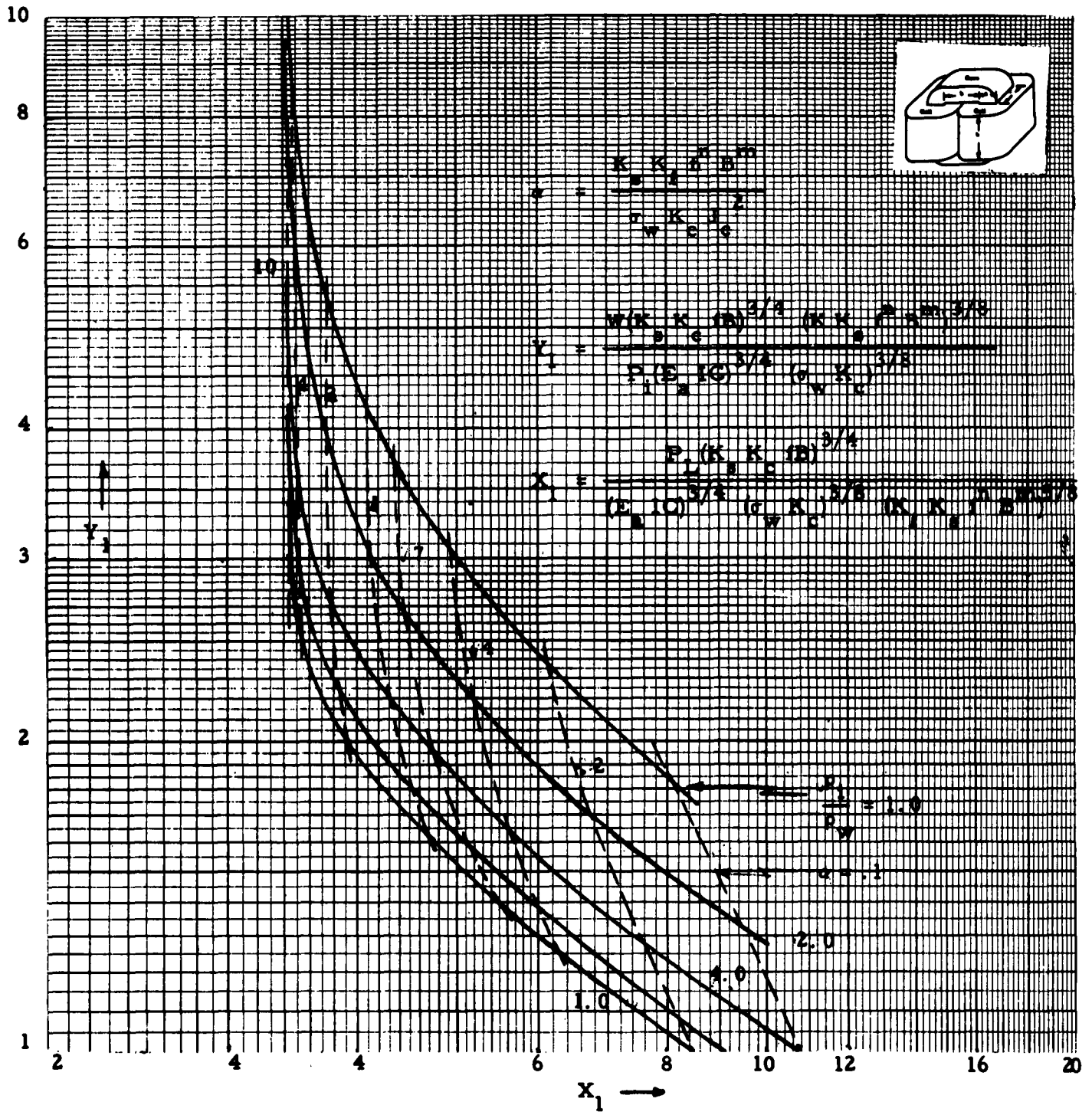
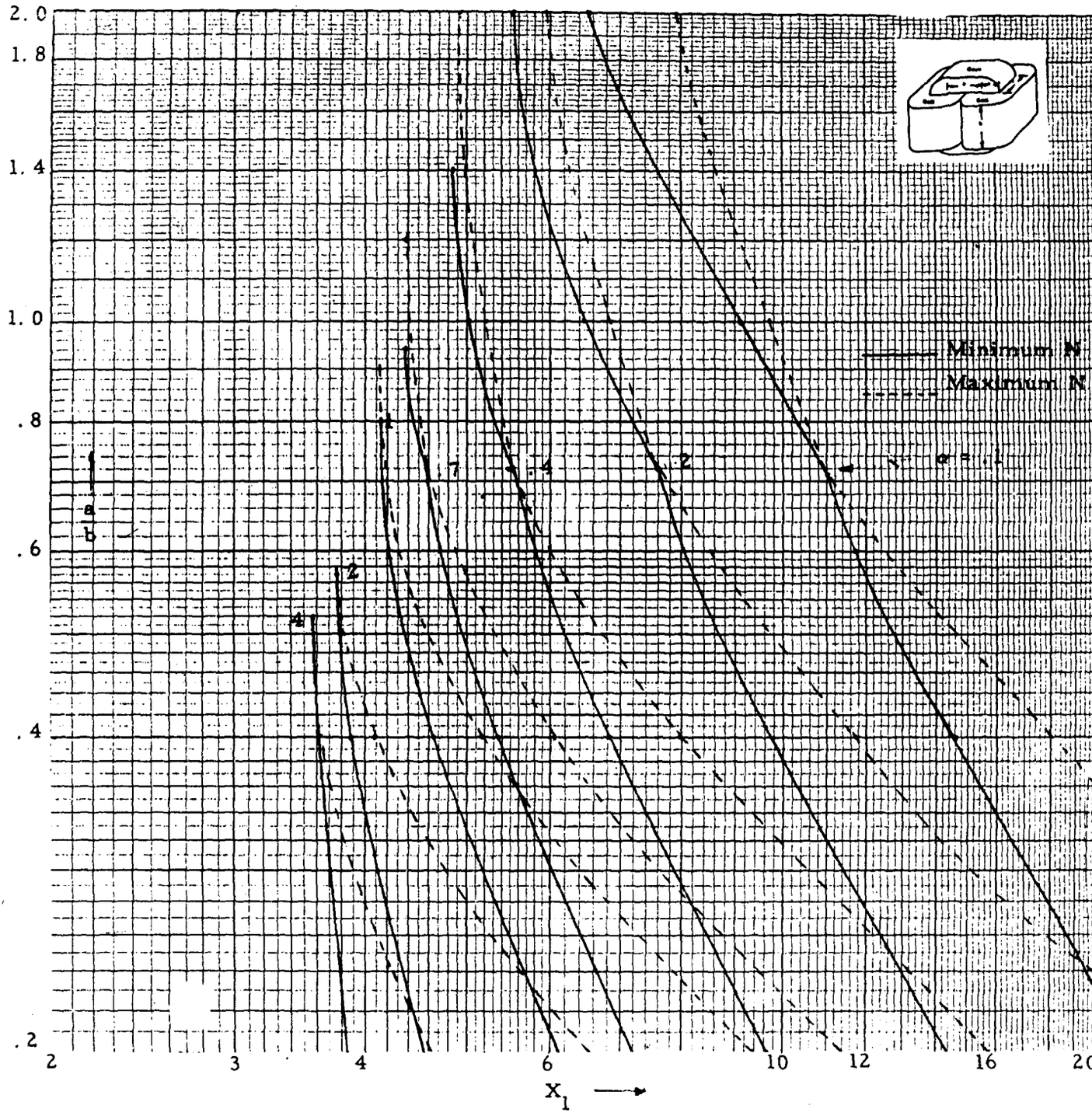


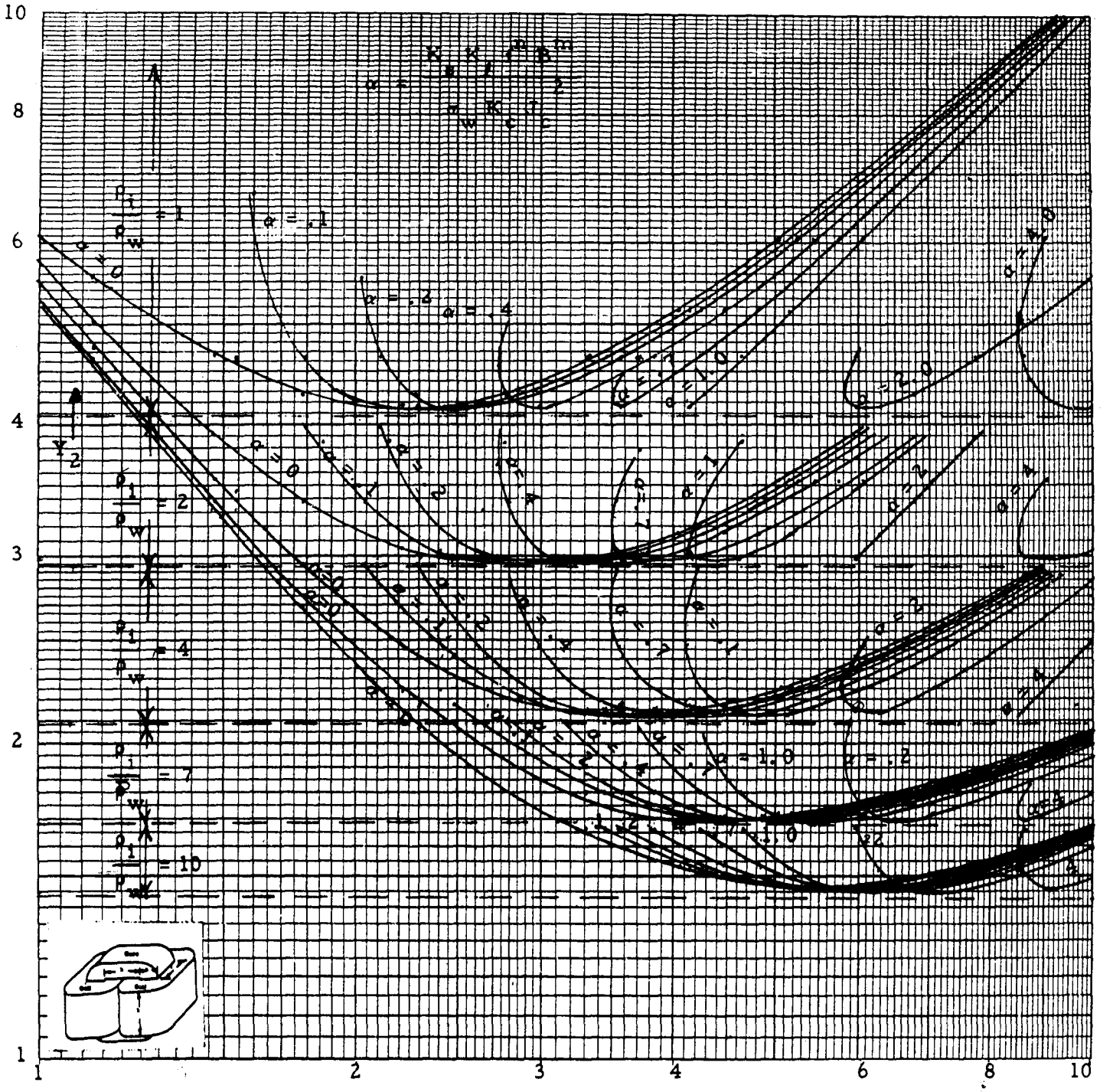
Figure 5.6-3: Ratio Core Leg Width to Window Width for a Minimum Weight Transformer with a Given Power Loss



$$\alpha = \frac{K_s K_\ell f^n B^m}{\sigma_w K_c J_c^2}$$

$$X_1 = \frac{P_L (K_s K_c fB)^{3/4}}{(E_a IC)^{3/4} (\sigma_w K_c)^{3/8} (K_\ell K_s f^n B^m)^{5/8}}$$

Figure 5.6-4: Minimum Weight as a Function of Power Loss, Magnetic Flux, Density Change, Current Density, Core Density, and Coil Density



$$Y_2 = \frac{W(K_s K_c fB J_c)^{3/4}}{P_i (E_a IC)^{3/4}}$$

$$X_2 = \frac{P_L(K_s K_c fB J_c)^{3/4}}{(E_a IC)^{3/4} (\sigma_w J_c^2 K_c)}$$

Figure 5.6-5 Ratio of Core Leg Width to Window Width for a Minimum Weight Transformer for a Given Power Loss

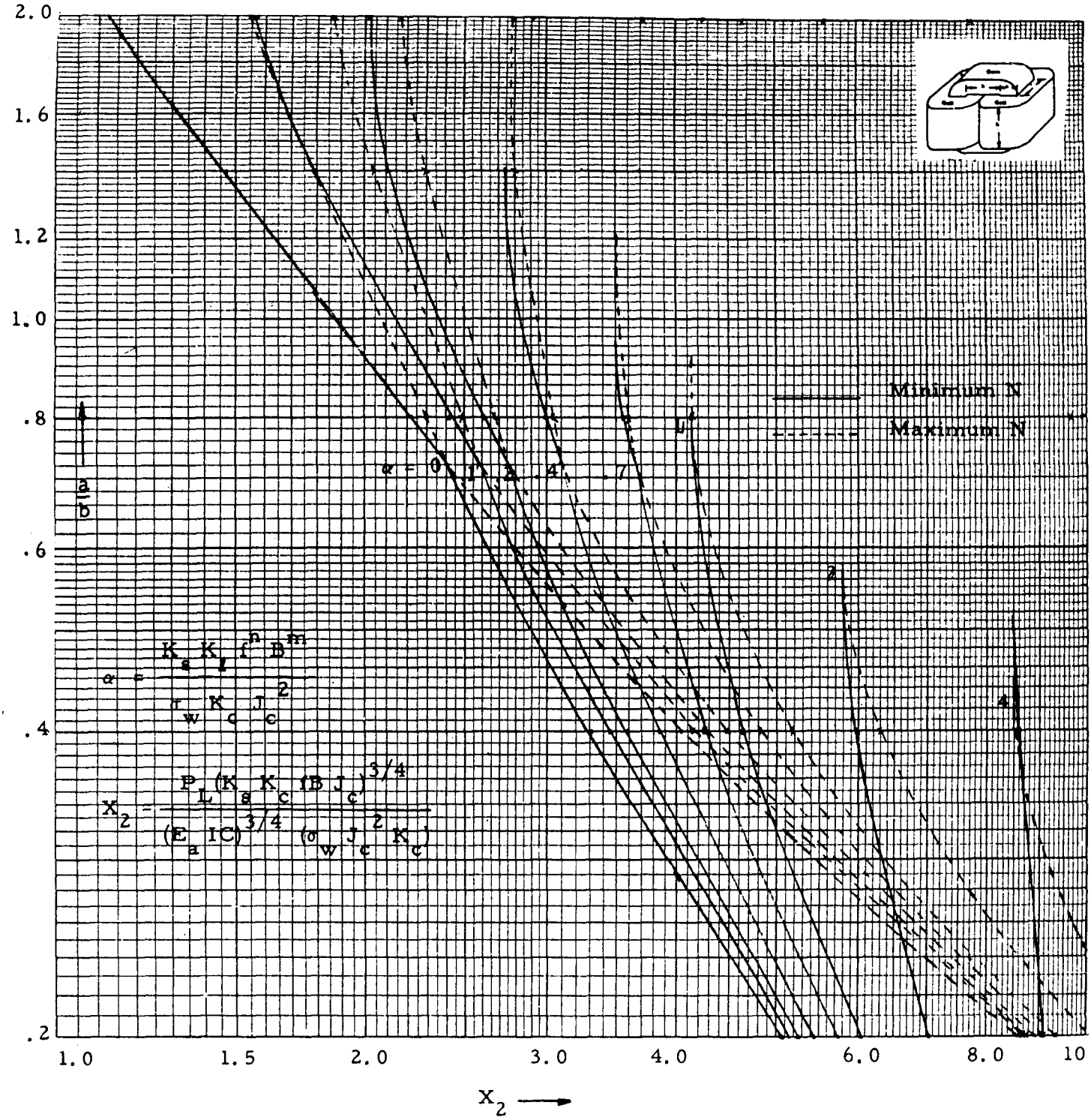


Figure 5.6-6: Number of Turns on Chosen Coil of Minimum Weight Transformer as a Function of Ratio of Core Leg Width to Window Width

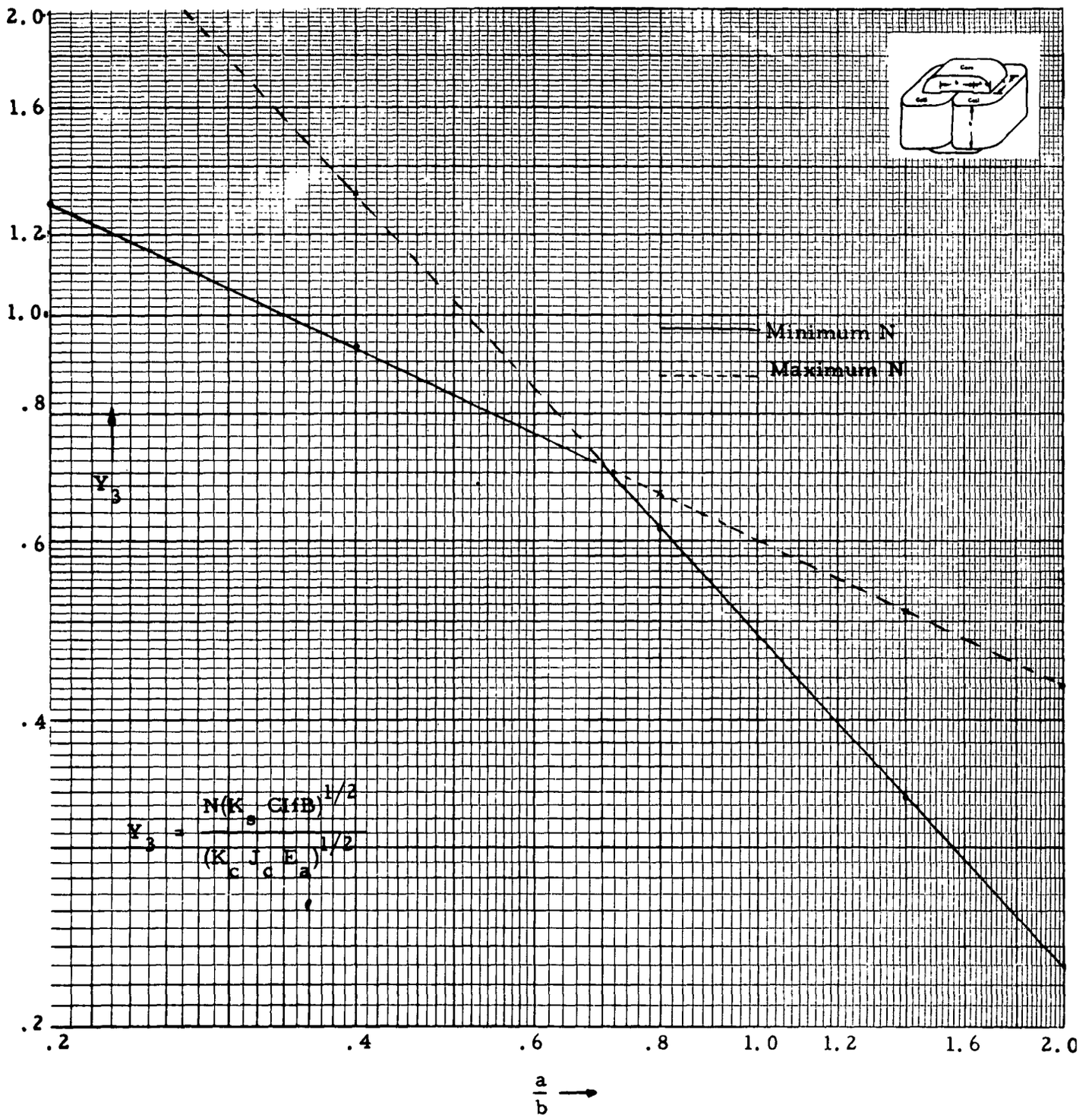


Figure 5.6-7: Dimension "b" of a Minimum Transformer as a Function of "a/b"

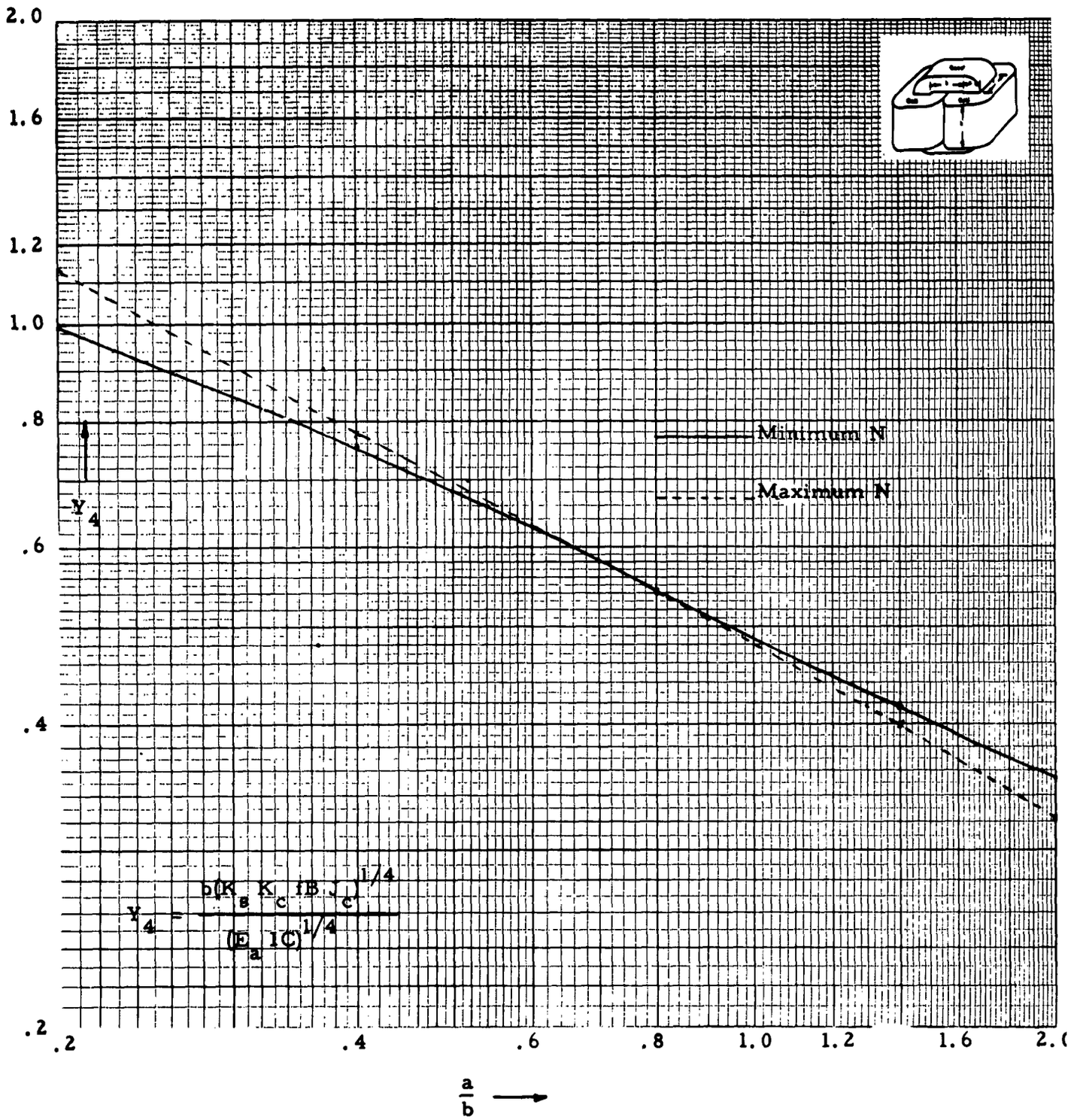


Figure 5.6-8: Minimum Possible Transformer Weight as a Function of Core Density, Coil Density, Magnetic Flux Density, and Current Density

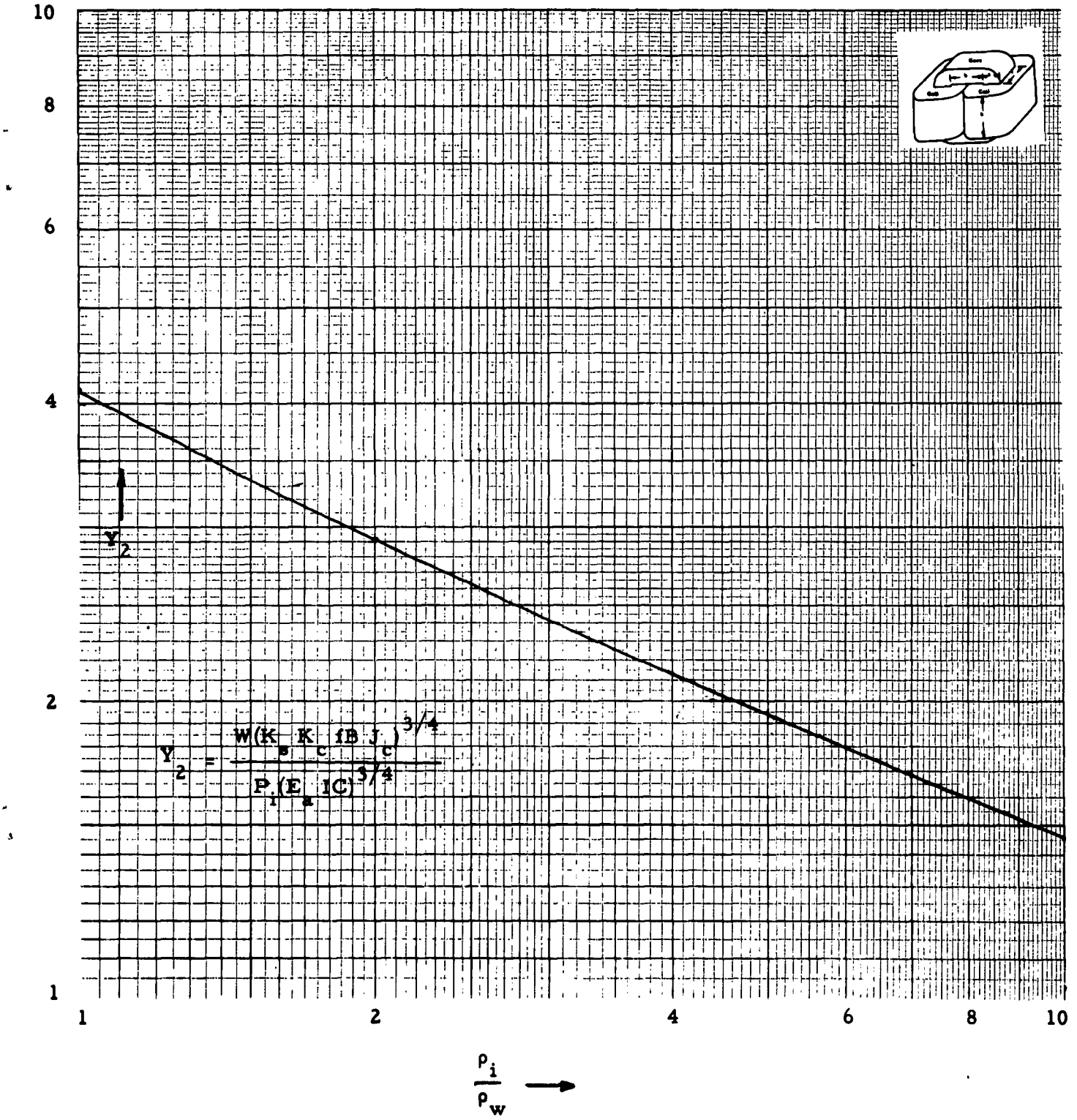


Figure 5.6-9: Power Loss of the Minimum Possible Weight Transformer as a Function of Core Density, Coil Density, Magnetic Flux Density, and Current Density

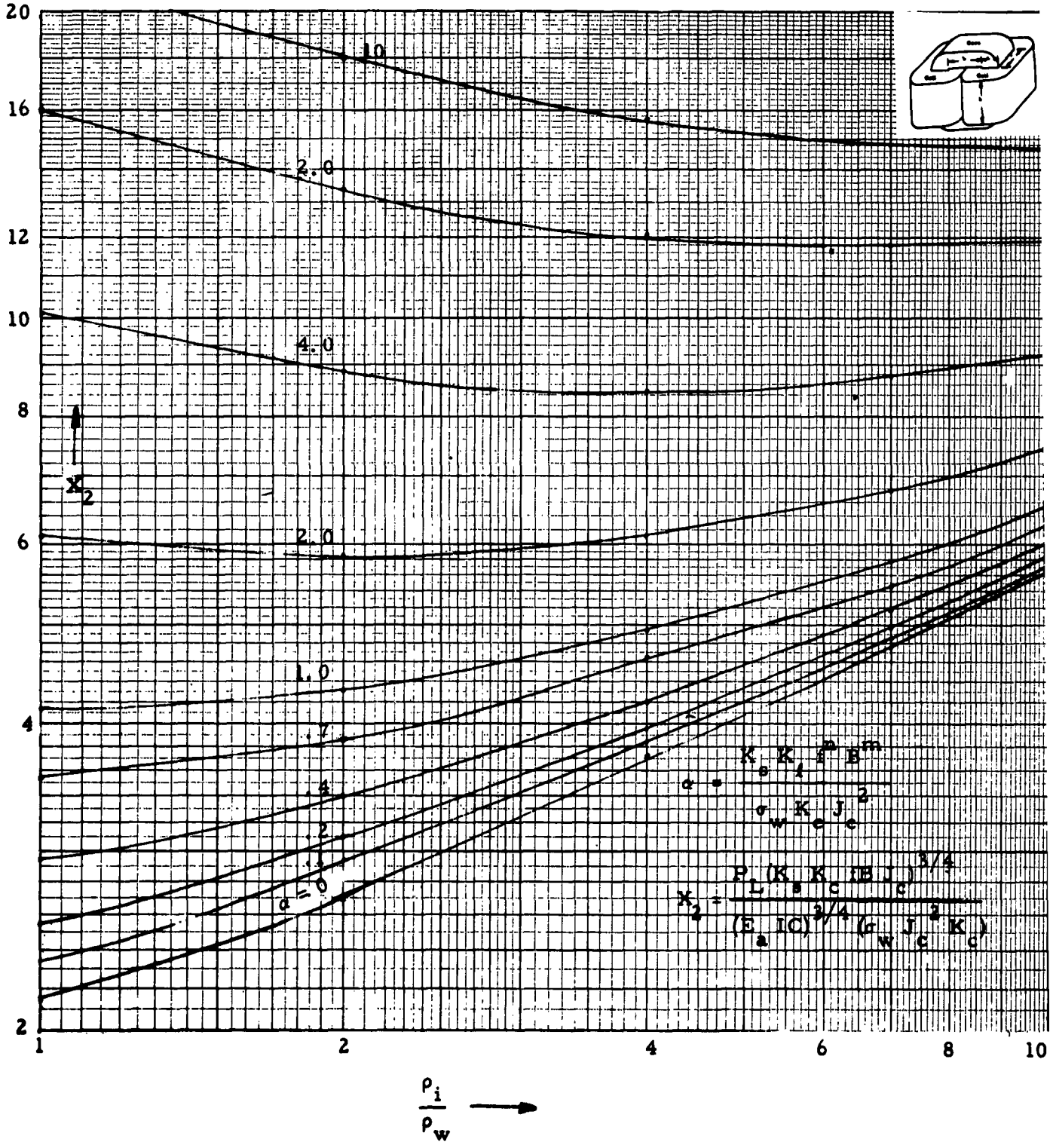


Figure 5.6-10: Weight of a Minimum Power Loss Transformer as a Function of Core Density, Coil Density, Magnetic Flux Density, and Current Density

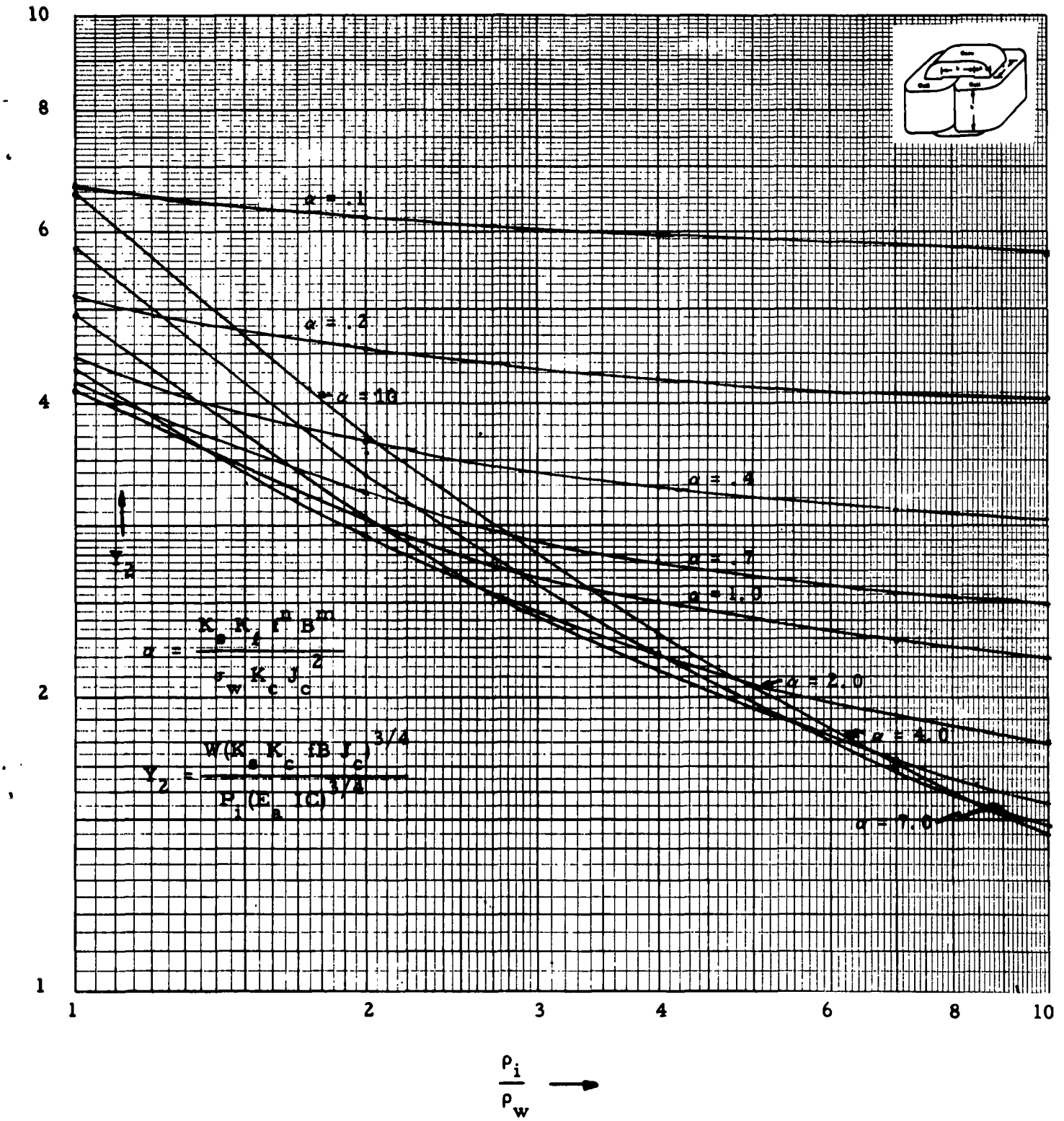


Figure 5.6-11: Minimum Possible Power Loss as a Function of Core Density, Coil Density, Magnetic Flux Density, and Current Density

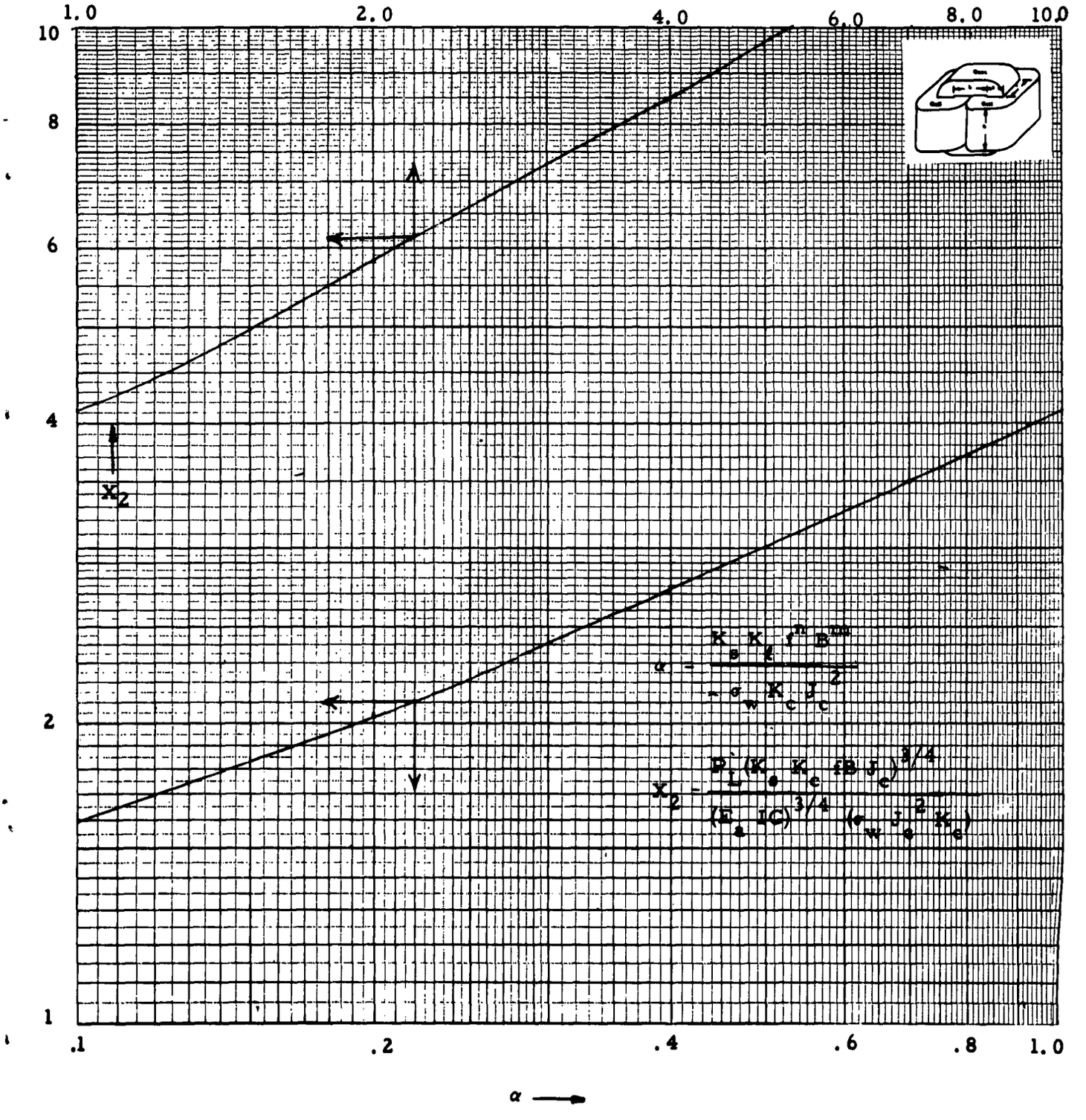
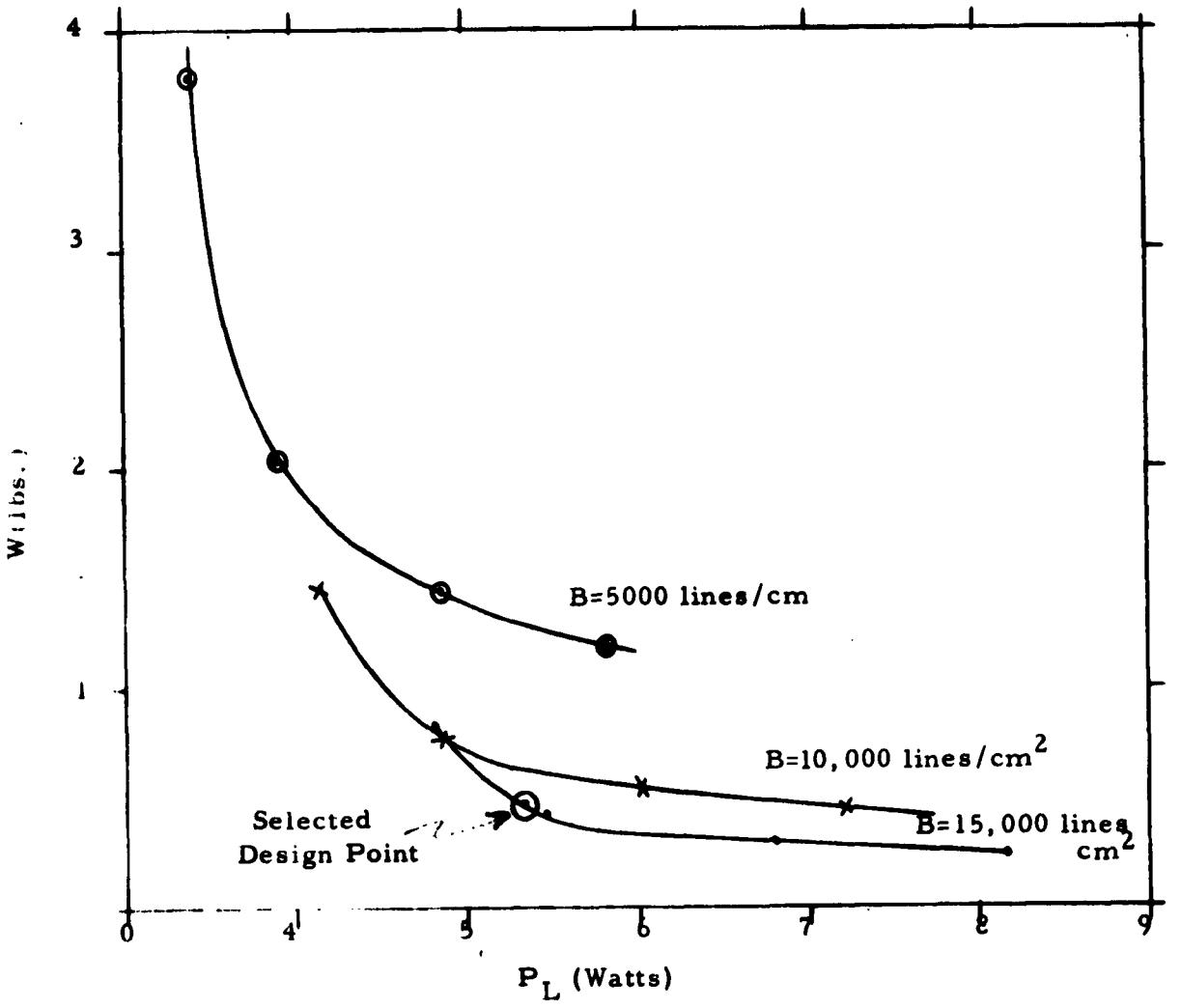


Figure 5.6-12: Minimum Weight Versus Power Loss Characteristics For a Two Winding, 400 cps, 100 Volt-Ampere Transformer.



6.0 TECHNICAL PROGRESS - SYSTEMS TASK

An end result of this study will be an indication of the make-up and performance characteristics of the optimum unconventional generator systems. Thus, the optimum combination of source voltage control and external voltage regulation for given types of applications will be indicated. In addition, the influence of source voltage level on the overall performance characteristics will be given. The purpose of the systems task is to evaluate the characteristics (weight, volume, efficiency, etc.) of various systems, and from this information, determine the optimum system. The systems effort will use the performance information generated in the power source portion and in the external voltage conversion and regulation portion of the overall study. In performing the systems evaluations an attempt will be made to arrive at simplified techniques for optimizing overall systems.

A second aspect of the systems task is a study of interaction problems existing between the unconventional generator and the voltage converter. These include the problems of system stability; filtering between power source and converter-regulator, and transient response.

A third aspect of the systems task is the overall system evaluation testing involving fuel cell power sources and the various external voltage converters being developed as part of this study. The intent of this systems testing is to confirm the previously predicted characteristics for the system.

To date, no effort has been devoted to the systems task. Effort will be applied when more information becomes available from the power source investigation and from the external voltage and regulation conversion investigation.

7.0 PLANNED ACTIVITY FOR THE NEXT REPORT PERIOD

7.1 Power Source Investigation

During the next reporting period, the effort in the power source investigation area will be devoted to the study of fuel cell dynamic electrical characteristics. The test approach will be planned in detail and a test set-up established. Careful attention will be given to having a test approach which will permit rapid evaluation of any fuel cell.

7.2 External Voltage Conversion and Regulation

During the next reporting period, activity will continue in the three areas of investigation discussed in this Progress Report, namely:

1. Flyback Circuit Development
2. High Frequency Switching Investigation
3. Advanced Device Investigation

In addition, Task 3, which is devoted to AC wave shaping techniques, will begin.

The completion of the flyback circuit development will involve changes in the design of the power transistor drive circuit and closing the loop to maintain a regulated DC output voltage. A comprehensive evaluation of the circuit will be completed to determine actual performance with respect to theoretical calculations. This work will be done independently from the power source. After the completion of these tests, it is anticipated that the circuit will be optimized and fabricated for final evaluation with a fuel cell power source.

In the high frequency switching investigation, the work associated with the study of transformer configurations and losses will continue. At the completion of that portion of the study, effort will continue to be directed toward a component examination which will include weight and power loss relationships as a function of frequency. Solid state devices will be treated, along with dielectric elements and various materials uniquely adapted to high frequency operation. It is also planned to begin work involved in the overall circuit concepts associated with high frequency operation.

In the advanced device investigation, the initial study and survey of power transistor will continue in the direction of testing commercially available devices. In addition, an effort has begun to construct or fabricate devices which will meet the specifications developed. At the present time, it is anticipated that devices will be constructed on a laboratory model basis using known and existing techniques but modifying basic design concepts. In addition, it is planned to conduct a preliminary examination of other unique switching devices with respect to circuit concepts and configurations. Those devices which appear attractive will be further explored in terms of obtaining measurements and preliminary laboratory tests.

During the next reporting period, work will begin on the AC wave shaping techniques study. The preliminary effort will be devoted to analytical and circuit studies to determine the most feasible approach with respect to the mode of operation, range of power levels, and source voltage levels which are of interest in this study. It is anticipated to have a categorized assessment of multiple pulse width modulation in comparison to stepped wave modulation. In addition, other means of wave shaping will be explored.

7.3 Systems Task

No effort is planned in systems area during the next reporting period.

8.0 REFERENCES

1. Magnetic amplifiers (book) by Dr. H.F. Storm. Published by Wiley & Sons, Inc. New York, N.Y.

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5. "SCT - Transistor Power Control Using Inhibit Turn Off" by R.E. Morgan, General Electric Patent Docket No. 14D-2725.